

**Three Dimensionally Interconnected Silicon Nanomembranes for
Optical Phased Array (OPA) and Optical True Time Delay (TTD)
Applications**

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Dr. GernotPomrenke

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Lead Principal Investigator:
Ray T. Chen

The University of Texas at Austin
MURI Website:

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Summary of Accomplishments

1. We present an experimental demonstration of an optical phased array implementation on silicon nanomembrane. The integrated on-chip array configuration is non-uniform and avoids grating lobes inside the field of view during beam steering while allowing the waveguide separation to be large enough to prevent optical coupling. A 1x12 multimode interference beam splitter uniformly excites the arrayed waveguides. Individually controllable micro-heaters modulate the optical phase in the arrayed waveguides. A beam steering angle of 10.2° in a silicon planar guide equivalent to an effective steering angle of 31.9° in air is demonstrated at 1.55 μ m.
2. Design and fabrication of a 2x2 two-mode interference (TMI) coupler based on-chip polarization splitter is presented. By changing the angle between the access waveguides, one can tune the effective TMI length for the mode with less optical confinement (Transverse Magnetic, TM) to coincide with the target TMI length for a desired transmission of the mode with higher optical confinement (Transverse Electric, TE). The fabricated 0.94 μ m long 2x2 TMI splits the input power into TM (bar) and TE (cross) outputs with splitting ratio over 15dB over 50nm bandwidth. Fabrication tolerance analysis shows that the device is tolerant to fabrication errors as large as 60nm.
3. We have investigated the feasibility of multimode polysilicon waveguides to demonstrate the suitability of polysilicon as a candidate for multilayer photonic applications. Solid Phase Crystallization (SPC) with a maximum temperature of 1000°C is used to create polysilicon on thermally grown SiO₂. We then measure the propagation losses for various waveguide widths on both polysilicon and crystalline silicon platforms. We find that as the width increases for polysilicon waveguides, the propagation loss decreases similar to crystalline silicon waveguides. At a waveguide width of 10 μ m, polysilicon and crystalline silicon waveguides have propagation losses of 0.56dB/cm and 0.31 dB/cm, respectively, indicating there is little bulk absorption from the polysilicon and is the lowest propagation loss for polysilicon demonstrated to date. In addition, the first 1x12 polysilicon MMI is demonstrated with a low insertion loss of -1.29dB and a high uniformity of 1.07dB. These results vindicate the use of polysilicon waveguides of varying widths in photonic integrated circuits.
4. We present an on-chip vertically integrated three-dimensional photonic integrated circuit. Double-layer 1x12 multimode interference (MMI) couplers are fabricated on silicon membranes using double-bonded silicon-on-insulator wafers. The input light is transverse electric polarized operating at 1550nm. The top layer MMI coupler has an excess loss of 0.48dB and uniformity within 1.1dB. The bottom layer MMI coupler has an excess loss of 2.9dB and uniformity within 1.7dB.

5. We propose a novel platform for three dimensional photonics. A double layer 1x12 multimode interference coupler is fabricated based on transfer printing of silicon nanomembrane. Optical characterizations confirm low insertion loss and uniform outputs.
6. We demonstrate a single-step through-etched, grating couplers based on subwavelength nanostructures. The grating consists of arrays of 80 nm x 343 nm rectangular air holes, which can be patterned in a single lithography/etch. A peak coupling efficiency of 59 % at 1551.6 nm and a 3 dB bandwidth of 60 nm are achieved utilizing the silicon-on-insulator platform with a 1 μ m thick buried-oxide layer for TE (transverse electric) mode. The performance is comparable to gratings requiring much more complicated fabrication processes.
7. We have shown the design and experimental results as a proof of concept for a low loss and broadband on-chip spot size converter that can significantly reduce the insertion loss between a optical fiber and a silicon photonic chip. The spot size converter demonstrated has a 5dB coupling loss. This structure will create a better interface between a fiber and a silicon photonic chip, and help drive the implementation of silicon photonics technology in areas such as optical communications and sensors.
8. We experimentally demonstrate highly efficient coupling into a slow light slotted photonic crystal waveguide. With optical mode converters and group index tapers that provide good optical mode matching and impedance matching, a nearly flat transmission over the entire guided mode spectrum of 68.8nm range with 2.4dB minimum insertion loss is demonstrated. Measurements also show up to 20dB baseline enhancement and 30dB enhancement in the slow light region, indicating that it is possible to design highly efficient and compact devices that benefit from the slow light enhancement without increasing the coupling loss.
9. We demonstrate a four-channel on-chip true-time-delay module based on a photonic crystal waveguide array. Using the photonic crystal taper to minimize the coupling loss, the delay lines with 1~3mm long photonic crystal waveguides can operate up to a group index $n_g \sim 23$ without significant loss. The large group velocity dispersion enables continuous and wavelength-tunable time delays. Measurements show a highly linear phase-frequency relation, highest time delay up to 216.7ps, and large tuning ranges of 58.28ps, 115.74ps, and 194.16ps for 1~3mm delay lines. The chip-scale true-time-delay module occupies only 0.18mm² area and can provide $\pm 44.38^\circ$ steering for an X-band phased-array-antenna.

1.0 1x12 Unequally-spaced Waveguide Array for Actively-tuned Optical Phased Array on a Silicon Nanomembrane

Traditionally, optical beam steering has been achieved through mechanically controlled MEMS system [1] and liquid crystal (LC) based optical phased arrays (OPAs) [2-4]. While mechanical beam steering provides high steering efficiency and relatively large scanning angles, high precision rotating stages are required, which increase the device complexity and are not fast enough for high speed applications. LC OPAs are capable of beam steering without expensive and complex mechanical systems but suffer from low steering speed ($\sim 10\text{ms}$) and limited steering angle ($<10^\circ$) [4]. Also, increased steering angle causes degradation of the side-lobe level (SLL) and prohibitively coarse angular resolution [5]. OPAs can also be implemented using waveguide arrays. A 2-element waveguide array on GaAs with GHz steering speed was demonstrated with a maximum steering angle of $\sim 6^\circ$ [6]. A thermo-optically controlled waveguide array fabricated on silicon-on-insulator (SOI) demonstrated a steering angle of 2.3° at a wavelength of 1550 nm [7].

For uniform OPAs capable of large angle beam steering, an inter-element spacing of about one-half the operating wavelength is required which would result in strong coupling between adjacent waveguides in the array. In order to overcome this trade-off between the maximum steering angle and waveguide spacing for linear uniform arrays, we proposed a non-uniform array consisting of uniform sub-arrays with non-overlapping grating lobes [5]. Also, compared to a uniform array with half-wavelength spacing, the larger total aperture of such an array results in narrower beam width in the far field, which is advantageous for scanning applications [5]. In this letter we report the implementation of a non-uniform optical array for large angle beam steering.

A schematic of the OPA device on SOI is shown in Figure 1(a), showing both photonic and electronic layers vertically separated by a layer of silicon dioxide for optical isolation. The beam propagation simulation of the photonic circuitry of Figure 1(a) at $\lambda=1.55\mu\text{m}$ is shown in Figure 1(b). The optical input power is uniformly divided into 12 waveguides using a 1x12 multimode interference (MMI) beam splitter, which has a width and length of $60\mu\text{m}$ and $553.4\mu\text{m}$, respectively. The input and output access waveguides' widths are $2.6\mu\text{m}$, which has been optimized for high MMI performance [8]. The MMI output access waveguides' widths are adiabatically tapered down to 500nm over $250\mu\text{m}$ length using a linear taper for single mode operation. Previously, we reported that this MMI coupler has an insertion loss of 1.13dB , and uniformity fluctuation within 0.72dB [9]. The input light is transverse-electrically (TE) polarized that provides higher optical mode confinement compared to the transverse-magnetic (TM) polarization for $500\text{nm} \times 230\text{nm}$ single mode silicon waveguides [Fig. 2(a)]. Also, due to the large index discontinuity at the top and bottom waveguide faces, the TM mode profile has larger vertical spread that reaches the micro-heaters and result in high propagation loss with a $1\mu\text{m}$ top cladding of SiO_2 .

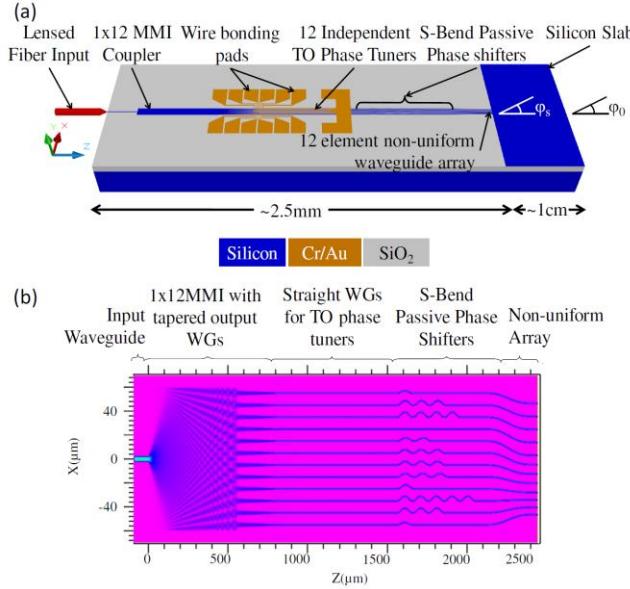


FIG 1-1.(a) A schematic of the silicon waveguide based optical phased array. (b) Beam propagation simulation of the photonic circuit.

There are 12 independently addressed 800nm wide and 500μm long thermo-optic (TO) phase modulators, as depicted in Fig. 1(a), to provide continuous phase tuning needed for beam steering. Independent phase shifterns enable us to reset with modulo 2π phase shifts ($2m\pi + \Delta\theta_n = \Delta\theta_n$, where m is a positive integer and $\Delta\theta_n$ is the phase shift of the n^{th} element) [10]. The following passive s-bend phase shifters [Figure 1(b)] compensate for the quadratic MMI beam splitter output phase profile [11] and change the separation of the uniform MMI outputs to that of the non-uniform array. This phase compensation allows the output beam to be steered at 0° when no heat is applied to the 12 phase shifters. The waveguides are then arranged in a non-uniform 12-element array, consisting of 3 four-element uniform sub-arrays, as shown in Figure 2(a). The spacing of each i^{th} sub-arrays s_i is chosen such that there is no overlap of its far-field grating lobes with those of the other sub-arrays [5]. The smallest inter-element spacing is 3.1μm and the total array size is $A=46.5\mu\text{m}$.

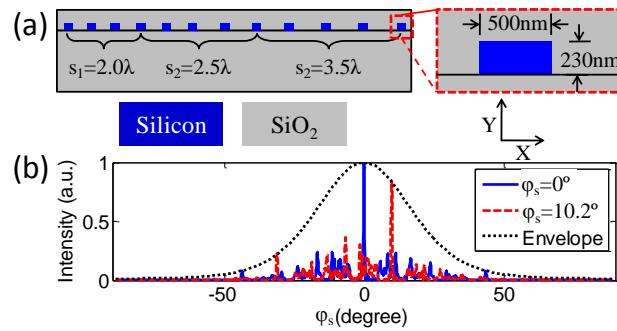


FIG 1-2. (a) 12-element non-uniform array design with 3 sub-arrays of single-mode silicon waveguides embedded in silicon dioxide, with dimensions of a single waveguide shown in the inset. (b) Theoretical far-field pattern for a non-steered and a steered beam inside the planar guide. The envelope is the far field pattern of a single silicon waveguide embedded in silicon dioxide.

The OPA output waveguides are terminated at a 1cm long silicon planar guide, in which the interference of the light from the 12-channel array results in beam steering at the far field zone. The steering angle is observed along the exit side of the planar guide at the chip edge [Figure 1(a)]. For the far field condition to be satisfied, $n_{\text{eff}} A^2 / (D\lambda) < 1$ is required [12], where A is the aperture size of the OPA, λ is the operating wavelength, and D is the distance of the observation point from the array (here the length of the silicon planar guide), and n_{eff} is the effective refractive index of propagation inside the silicon slab.

Similar to the uniform array, the non-uniform array is linearly phased, that is for any n^{th} array element, $\gamma_n / |\overline{d}_n| = r$, where γ_n is the phase applied to the n^{th} element, \overline{d}_n is the position vector of the n^{th} element, and r is a constant. The steering angle inside the silicon planar guide is given as $\varphi_s = \arcsin(\omega \sqrt{\mu \epsilon_{\text{eff}}} / r)$.

Note that as the beam reaches the end of the slab and enters free space, its direction is governed by Snell's Law. The theoretical far field patterns for steered and non-steered beams are shown in Figure 2(b).

We used SOI from SOITEC with 3 μm buried oxide (BOX) and 250nm top silicon layer, which is thermally oxidized to create an oxide etch mask, leaving a final silicon thickness of 230nm. Electron beam lithography and reactive ion etching is used to pattern this layer to form the photonic circuitry. A scanning electron microscope (SEM) picture of the interface between the unequally spaced OPA and silicon nanomembraneplanar guide is shown in Figure 3(a). Using the Plasmatherm 790, a 1 μm thick film of plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide (325°C, 80W, 400mTorr, 42sccm N₂O, 21sccm SiH₄) was deposited as top cladding, which is sufficient to isolate the TE guided modes from the electrodes to prevent high optical loss. Metal heaters are patterned over the waveguides by e-beam lithography and thermal evaporation and liftoff of 150nm of Cr/Au [10/140] film. An optical microscope picture of the heaters aligned over the output waveguides and 12 bonding pads is shown in Figure 3(b).

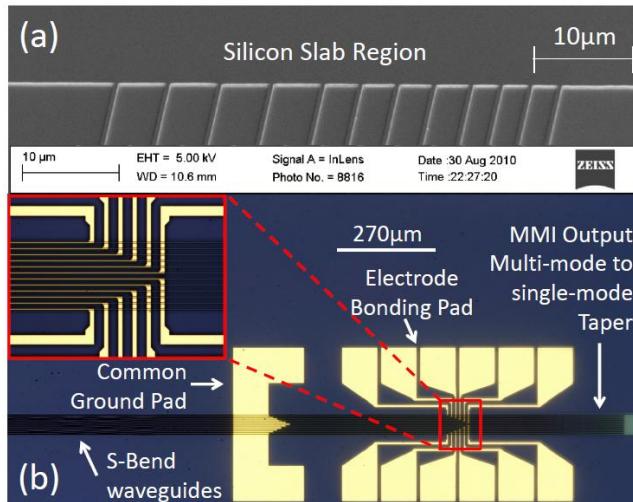


FIG 1-3. (a) Tilted SEM view of the unequally spaced OPA output and silicon nanomembraneplanar guide. (b) Optical microscope picture of the 12 thermo-optic heaters with bonding pads.

We engineered the “bread loafing” effect in which self-aligned voids are formed during PECVD oxide deposition, and are shown in Figure 4(a). COMSOL Multiphysics simulations in Figure 4(b) indicate the effectiveness of these voids in directing the generated heat toward the silicon waveguides by reducing lateral heat transfer, and therefore reducing the required power for phase shifting. To accurately characterize the phase perturbations of the thermo-optical modulators, we fabricated Mach-Zehnder (MZ) modulators alongside the OPA devices with dimensions identical to the OPA with regard to waveguide and heater geometry. We experimentally confirmed a switching power of $P_{\pi}=12.4\text{mW}$ along with a switching time of $9.8\mu\text{s}$ which corresponds to a steering speed of 100kHz .

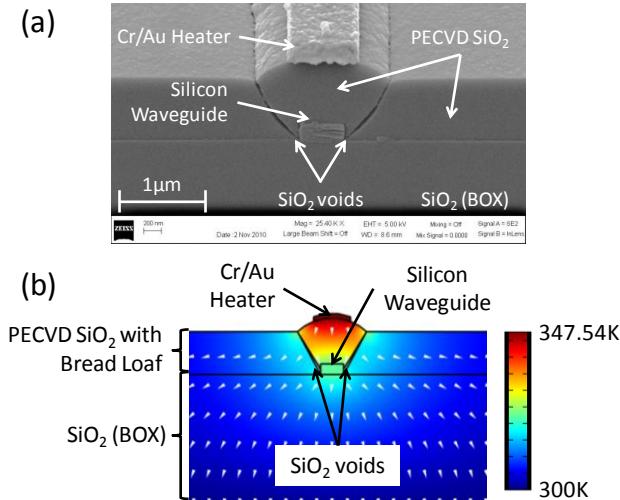


FIG 1-4. (a) SEM cross section of a heater over its waveguide. (b) COMSOL Multiphysics simulation of the thermal profile of the microheater and waveguide cross section with bread loafing of the oxide.

TE polarized light at 1550nm from a polarization maintaining lensed fiber (PMF) with a $2.5\mu\text{m}$ output mode diameter was coupled into the input waveguide. An infrared (IR) camera connected to a variable objective lens captured the top-down far field image at the end of the silicon planar guide.

For active beam steering, we first set the input voltages to thermo-optically modulate the array phases in such a way that the electrical power applied to the micro-heaters, and therefore the applied phase shift of the corresponding array element, is linearly proportional to the distance of the element from the origin. Figure 5(a) demonstrates the measured beam steering angle at the edge of the silicon planar guide, along with the theoretical steering angles as a function of the electrical power to the outermost array element, which needs the largest phase shift. The required electrical input power is calculated using the phase shift data from the MZ test. As shown in Figure 5(a), when the steering angle increases, the power required for beam steering without reset becomes prohibitively large for our voltage source and limits us to a steering angle of 2.5° inside the silicon planar guide. Figure 5(a) also shows beam steering angles achieved with reset by applying modulo 2π phase shifts to the independently controlled electrodes. We were able to steer the beam at 10.2° inside the silicon planar guide equivalent to an effective angle of 31.9° in air as predicted by Snell’s Law, with SLL better than -3dB , while limiting the maximum power per channel to less than $P_{2\pi}=24.8\text{mW}$.

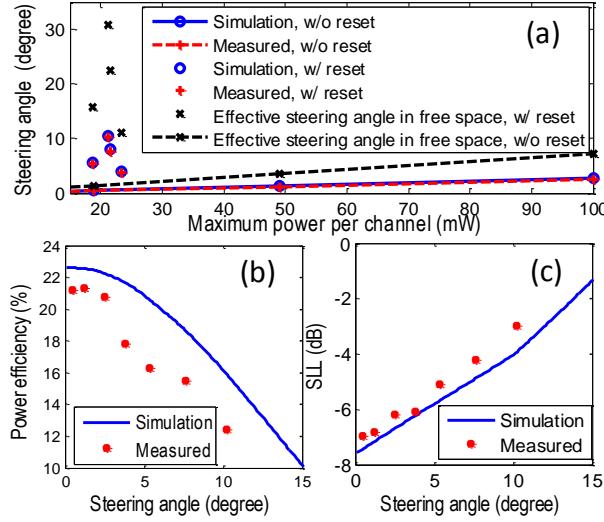


FIG 1-5.Far field characterization, (a) simulated and measured steering angle versus maximum power per channel. Effective steering angles in free space are determined from measurement data. (b) Power efficiency versus steering angle, (c) side-lobe-level versus steering angle.

Using a similar technique as [12], the OPA far field is observed and is used to characterize its output performance. Figures 5(b) and 5(c) demonstrate the OPA performance characterization based on the power efficiency and SLL as functions of the measured steering angle, respectively. The power efficiency is calculated by integrating the intensity over the angle interval that constitutes the main lobe (within $1/e^2$ of the maximum beam intensity). The resulting is then normalized to intensity integrated over -90° to $+90^\circ$. From the simulations, we expect -4dB SLL at 10.2° . The degradation in the performance is due to the variation in $P_{2\pi}$ of the micro-heaters, which results in increasing inaccuracies in the applied phase shift as the number of resets increases at larger steering angles. Using the effective index of the planar guide, $n_{eff} = 2.9$, we determine that the 10.2° steering in the planar guide corresponds to a steering angle in free space of 31.9° .

In summary, using a silicon nanomembrane based unequally spaced 1x12 waveguide array for actively tuned OPA that relaxes the strict waveguide spacing requirement for large angle beam steering, we have demonstrated a steering angle in free space of 31.9° at $1.55\mu\text{m}$ wavelength. Our optical beam steering system is fabricated on SOI using CMOS compatible processes. Phase modulation is achieved thermo-optically via the use of thin-film metal heaters that are independently controlled. We have demonstrated that low-power optical beam steering is possible by applying modulo 2π phase shifts to the independently controlled electrodes. The steering speed is determined by the TO phase shifting mechanism and is 100KHz using the TO effect, which is 2 orders of magnitude larger than LC OPAs.

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2.0 Ultra-compact and Fabrication-Tolerant Integrated Polarization Splitter

On-chip polarization splitters (PSs) are key components of integrated photonic circuits that consist of polarization-dependent devices [1]. Interference-based passive PSs provide low-loss operation and high polarization splitting ratio (SR), and can be designed for single etch step fabrication [2]. The interference-based PSs that have been demonstrated thus far, utilize either directional couplers [2][3], or multimode-interference couplers (MMIs) [4][5].

Symmetric directional coupler based PSs can be shortened ($\sim 100\mu\text{m}$) by reducing the gap between the coupled waveguides [3]. However, this also degrades the device fabrication tolerance, and potentially lowers its SR. Non-symmetric directional couplers can be designed to allow only one of the modes (TE or TM) to couple out of the input waveguide. The device fabrication tolerance can be improved by waveguide tapering [2]. However, this technique assumes linear design conditions that require relatively large gaps and thus, due to long coupling lengths, the resulting devices are $\sim 1500\mu\text{m}$ long [2].

In MMI based PSs, TM and TE polarizations can be split into different bar or cross states using the difference in their self-imaging beat-lengths, $L_\pi = \pi/(\beta_0 - \beta_i)$, where β_n is the n^{th} mode propagation constant supported by the multimode section [6]. In order to avoid long MMIs due to small beat-length differences of TM and TE polarizations, the required MMI length can be shortened by use of four-mode interference couplers [4], and further by use of two-mode interference (TMI) couplers [5].

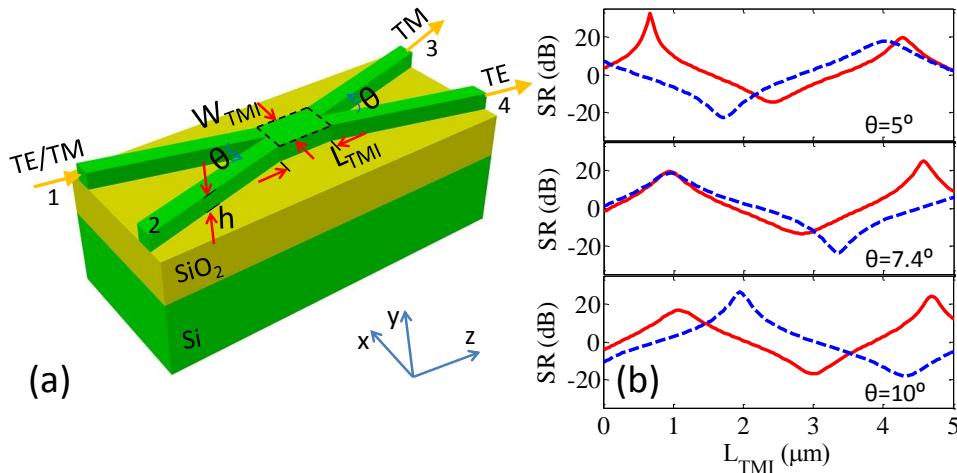


Fig. 2-1.(a) A schematic of the polarization splitter device. (b) Variations of P4/P3 and P3/P4 for input TE (solid red line) and TM (dashed blue line) polarized light, respectively, at different θ values, for $W_{TMI}=900\text{nm}$ and $h=230\text{nm}$ at $\lambda=1550\text{nm}$.

In order for a TMI to function as a polarization splitter, the TMI length (L_{TMI}) is chosen to be simultaneously equal to an odd (even) multiple of L_π for the TE polarization (L_π^{TE}) and an even (odd) multiple of L_π for the TM polarization (L_π^{TM}). A PS device on silicon-on-insulator (SOI) with L_{TMI} (not including the access waveguides) as short as $8.8\mu\text{m}$ has been demonstrated [5]. However, the resulting TMI is still several beat-lengths long. Since the fabrication tolerance and optical bandwidth of MMI devices are inversely proportional to their length [7], it is beneficial to reduce the TMI length to its

absolute minimum, one beat-length. In this letter, we report the design and fabrication of a one-beat-length long TMI based PS.

A schematic of the proposed TMI based PS on SOI is shown in Fig. 1(a). The thicknesses of the oxide and top silicon layers (h) are 3 μm and 230nm, respectively. A TMI width $800\text{nm} < W_{TMI} < 950\text{nm}$ supports only two TE and two TM modes, suitable for TMI operation [8]. The input /output access waveguide width is $W_w = W_{TMI}/2$. For a TMI, the output power at port 3 and 4 normalized to input power at port 1 (port 2 is idle) is given as $P_3/P_1 = \sin^2(\pi L_{TMI}/2L_\pi + \varphi)$ and $P_4/P_1 = \cos^2(\pi L_{TMI}/2L_\pi + \varphi)$, where, the phase term, φ , is determined by the coupling between the two access waveguides at the input and output. Assuming fixed h , only W_{TMI} and L_{TMI} have been thus far considered as the design parameters while the effect of φ on the device operation has been ignored.

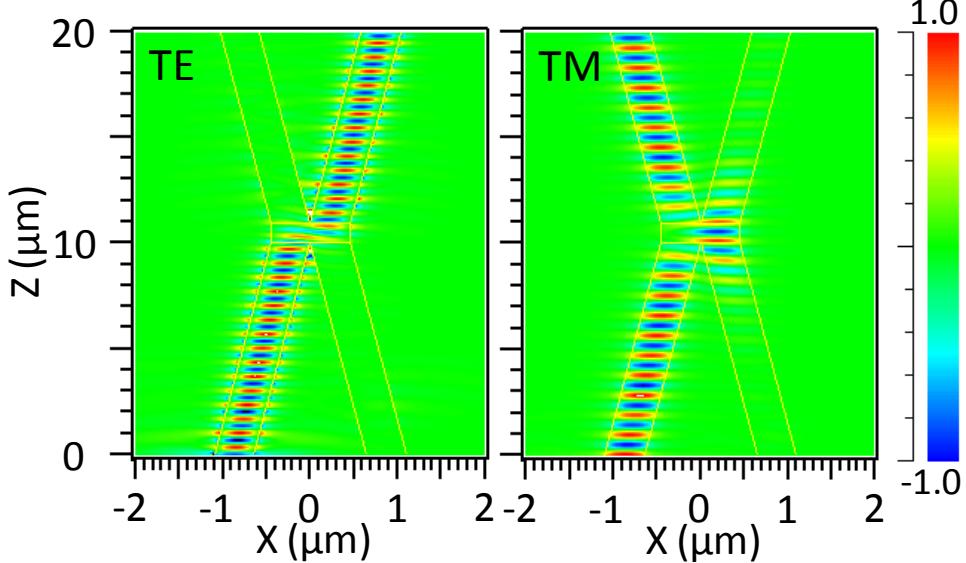


Fig. 2-2. FDTD Propagation field profiles for TE (Ex) and TM (Hx) input polarizations for $\theta=7.4^\circ$, $L_{TMI}=940\text{nm}$, $W_{TMI}=900\text{nm}$ and $h=230\text{nm}$ at $\lambda=1550\text{nm}$.

Assuming $W_{TMI}=900\text{nm}$, $h=230\text{nm}$ and wavelength, $\lambda=1550\text{nm}$, we simulate the device in Fig. 1(a) using the full vectorialeigenmode decomposition-based complex Film Mode Matching (FMM) solver (with 60 1D modes) of the FIMMPROP module. Fig. 1(b) shows the variations of power splitting ratio, P_4/P_3 and P_3/P_4 , versus L_{TMI} for input TE and TM polarizations, respectively. One notes that φ depends on both polarization and the angle between the access waveguides, θ . Also, for a TM polarized input, a change in θ has a considerably large effect on φ . This is not surprising, as the TM mode supported by the access waveguides is much less confined compared to the TE mode. Thus, for a TM input, the coupling between the two access waveguides is considerably stronger resulting in an effectively larger L_{TMI} that is more sensitive to θ than that for a TE input. Since the power splitting ratio changes much slowly with θ for a TE polarized input, the easily tunable θ can be used as a reliable design parameter for tuning the output SR.

Figure 1(b) shows that at $\theta=7.4^\circ$ and $L_{TMI}=0.94\mu\text{m}$, the 2x2 PS device operates in the cross and bar states for TE and TM polarized inputs, respectively. Note that $L_{TMI}=0.94\mu\text{m}$ is shorter than both $L_\pi^{TE}=1.80\mu\text{m}$ and $L_\pi^{TM}=2.31\mu\text{m}$. Fig. 2 shows the field propagation through this device from FDTD (RSoftTM) simulations,

which indicate that at $\theta=7.4^\circ$, $L_{TMI}=0.94\mu\text{m}$ effectively corresponds to $2L_\pi^{TM}$ and $1L_\pi^{TE}$. SR values for TE and TM inputs are $P4/P3=19.4\text{dB}$ and $P3/P4=18.6\text{dB}$, respectively. Insertion loss values for TE and TM inputs are $P3/P1=-0.25\text{dB}$ and $P4/P1=-0.35\text{dB}$, respectively.

Based on our simulation results the device performance becomes independent of the input/output access waveguide length when they are longer than $6.5\mu\text{m}$. Thus, the total device length, including the input/output access waveguides, is $13.94\mu\text{m}$. Ultracompact directional coupler based PSs with similar dimensions have been reported [9][10]. As discussed before, the fabrication tolerance remains an issue for short directional couplers with small gap sizes. In order to investigate the proposed PS fabrication tolerance, we assume that the fabrication errors appear as changes in waveguide width (ΔW) [2].

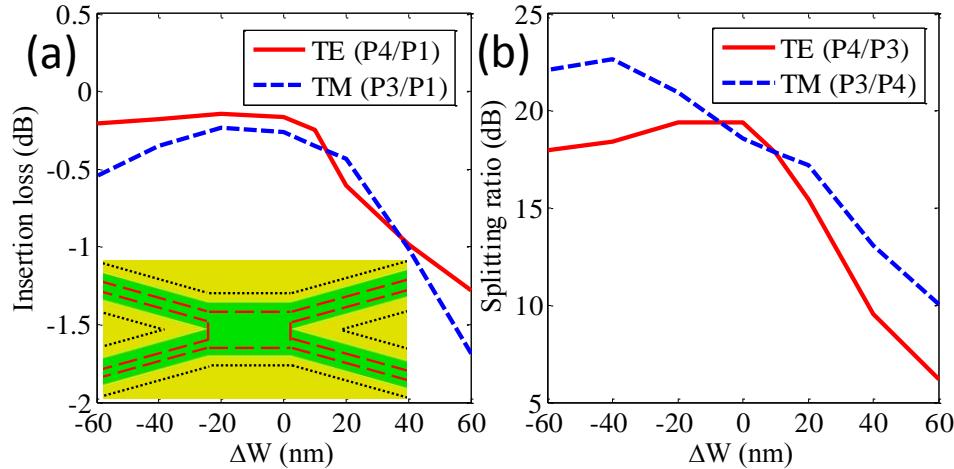


Fig. 2-3. Variations of (a) insertion loss and (b) polarization splitting ratios as functions of deviation in the waveguide width for input TE and TM polarizations. The inset of (a) shows a PS layout affected by $\Delta W < 0$ (dashed red) and $\Delta W > 0$ (dotted black).

The device layout changes due to $\Delta W < 0$ and $\Delta W > 0$ are depicted in Fig. 3(a) inset. A $\Delta W < 0$ does not change the TMI length while widening the gap between the access waveguides. When the waveguide width increases ($\Delta W > 0$), one can imagine that the *effective* TMI length increases but the *effective* gap between the access waveguides is just shifted away from the original TMI.

Variations of insertion loss and SR with ΔW for TE and TM polarized inputs are shown in Figs. 3(a) and (b), respectively. TM mode propagation in the access waveguides is near the mode cut-off, and a reduction in the waveguide width ($\Delta W < 0$) results in a significantly less confined modal field. Thus, in the case of TM input, the effect of wider gap due to $\Delta W < 0$ is compensated by the stronger coupling between the more spread-out modal fields. As the coupling at the access waveguides does not play a significant role for TE polarization, the PS device is tolerant to $\Delta W < 0$ for both TE and TM polarizations.

On the other hand, a $\Delta W > 0$ effectively increases the TMI length as $\Delta L = \Delta W / \sin(\theta/2) = 15.5 \Delta W$. In other words, $\Delta L / L \approx 15 \Delta W / W$. Note that for the self imaging process in the TMI to be tolerant to small changes in the TMI width, the changes in the (effective) TMI length must satisfy $\Delta L / L = 2 \Delta W / W$ [7]. Therefore, the large changes in the MMI length rapidly degrade the TMI performance for $\Delta W > 10\text{nm}$, for both TE and TM polarized inputs in a similar way. Note that for $\Delta W < 0$, the device fabrication tolerance is comparable to that of a tapered asymmetric directional coupler, which is nearly 500 times larger [2].

To benefit from tolerance to $\Delta W < 0$, we choose a fabrication process with a possible shrinkage in the waveguide width. For $\Delta W < 0$, the minimum distance between the access waveguides on each side is given as $\Delta W \cos(\theta)$. For $\Delta W < 0$, the tip shape between the access waveguides is blunt and does not introduce fabrication difficulties. The PS device is fabricated on Soitec SOI wafers consisting of 3 micron thick silicon dioxide and 250 nm thick top silicon device layer. The top silicon layer is oxidized to create a 45 nm top silicon dioxide layer, which serves as a hard mask in the silicon etch process.

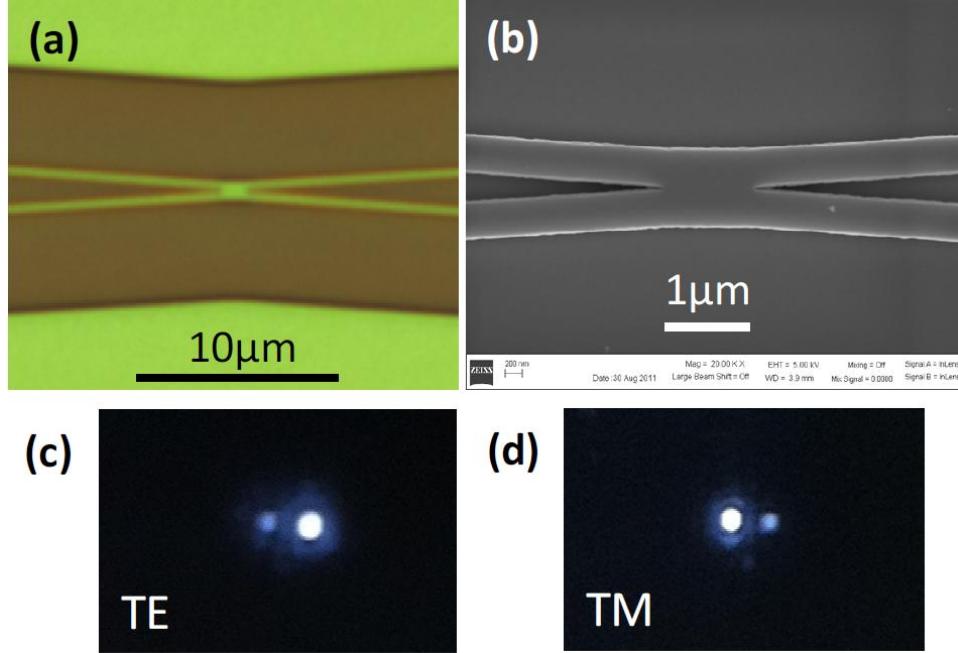


Fig. 2-4. Microscope (a) and SEM(b) images of the fabricated PS device. Top-down IR pictures of the PS outputs for TE (c) and TM (d) polarized inputs.

The oxidation process consumes 20nm of the top silicon layer and results in a final 230nm silicon layer. The top oxide layer is patterned using electron beam lithography and CHF₃/O₂ plasma based reactive ion etching (RIE). The pattern is then transferred to the silicon layer underneath by HBr/Cl₂ based RIE. In addition to a small etch undercut, due to the E-beam proximity effect, the area of the exposed positive resist (ZEP520) expands a little bit resulting in narrowing of the unetched areas of the top silicon layer. Overall, with this fabrication process, $\Delta W < 0$ is expected. Microscope and SEM images of the fabricated PS are shown in Fig. 4. Top-down SEM measurements indicate a final $\Delta W = -20\text{nm}$.

The PSs are tested on a Newport six-axis auto-aligning station. A broadband amplified spontaneous emission (ASE) source output light, covering 1520~1620 nm, is TE- or TM-polarized with an extinction ratio of over 30dB and butt coupled into/out of the input/output waveguide facets through a polarization maintaining lensed fiber. Top-down IR pictures of the outputs at the chip edge with TE and TM polarized input excitations are shown in Fig. 4.

Fig. 5 shows the spectra of normalized output power measured at Port 3 and Port 4, for TE and TM input excitations at Port 1. The results indicate polarization splitting ratios of P4/P3=18.2dB and P3/P4=16.8dB, respectively, for the TE and TM polarized inputs at $\lambda=1550\text{nm}$. The splitting ratio

remains better than 15dB over a 70nm bandwidth for the TE polarized input and over 50nm bandwidth for the TM polarized input. The TE and TM propagation losses in a fabricated 450nm x 230nm waveguide are estimated to be 7.5dB/cm and 16.3dB/cm, respectively, using a cutback technique, at $\lambda=1550$. In order to accurately estimate the device insertion loss, while excluding the input/output fiber/waveguide coupling loss and propagation losses in the access waveguides, we compare the transmission through two-stage cascaded TMIs with the transmission through a single TMI for each polarization. A narrowband laser ($\lambda=1550$) is used for insertion loss measurements. Our results indicate that the insertion loss is 0.8dB for the TE polarized input and 1.7dB for the TM polarized input.

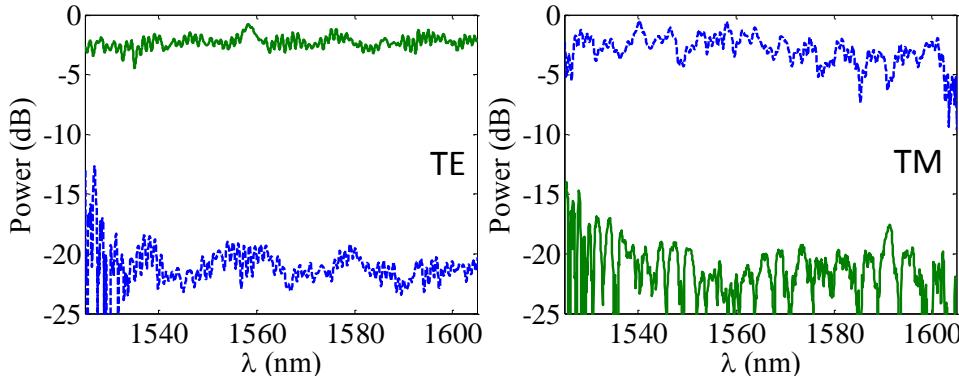


Fig. 2-5. Normalized output transmission spectra at P3 (dashed blue) and P4 (solid green) for TE and TM input excitations at P1. Data is normalized to the measured ASE output spectrum.

In summary, we presented the design and fabrication of a TMI based PS, for which the length of the TMI section is reduced to less than a single beat-length of the TE mode. While the device performance is sensitive to the angle between the two input/output access waveguides, the device is rather tolerant to width variations (shrinkage) in the TMI and the access waveguides. To the best of our knowledge, this TMI is the most compact and largest bandwidth self-imaging device demonstrated so far.

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3.0 Ultralow-loss polycrystalline silicon waveguides and high uniformity 1x12 MMI fanout for 3D photonic integration

1. Introduction

On-chip photonic networks are a promising solution for the interconnect bottleneck in high performance microelectronics. Crystalline silicon-on-insulator (SOI) is the most commonly used photonics platform due to its large index contrast with silicon dioxide ($\Delta n \sim 2.02$), which enables submicron waveguides and small bending radii. In addition, SOI exhibits excellent material properties such as low bulk absorption at telecom wavelengths and high electronic carrier mobility. While crystalline SOI is the most desirable, photonic devices would be restricted to the electronic layer. Furthermore, silicon photonics requires a thick Buried Oxide (BOX) layer (typically a few micrometers) for optical isolation from the substrate, but SOI for electronics requires a thin oxide layer ranging from tens to hundreds of nanometers to allow thermal flow into the substrate [Sherwood-Droz2011]. Although it has been shown that SOI for electronics can also be used for photonics [Holzwarth2008], it comes generally at the cost of more real estate and adds greater complexity and cost to the standard CMOS fabrication process. A multi-layer platform would enable photonic device versatility, as footprint and separation issues are mitigated.

In order to maximize such a platform's design flexibility, CMOS compatible silicon deposition methods are strongly desired. As it is not currently possible to deposit crystalline silicon, alternative materials must be considered. Silicon nitride is a low loss material that has been used for multilayer photonic integration [Sherwood-Droz2011], but its lower index contrast increases device footprint, and it also lacks any mechanism for high-speed modulation, limiting nitride solely to passive devices. Hydrogenated amorphous silicon deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) is a low loss material that has been used in multilayer stacks[Kang2011], but sufficient and stable hydrogenation of the silicon dangling bonds are critical to maintaining its low loss property. Zhu et al have demonstrated that the propagation loss for hydrogenated amorphous silicon waveguides starts to increase rapidly at temperatures above 300°C [Zhu2010], and Selvaraja et al have shown that the refractive index change measured from a Mach-Zehnder Interferometer (MZI) starts to occur at 200°C[Selvaraja2010]. In addition to thermal stability of hydrogenated amorphous silicon, another significant challenge is that the charge mobility is very low due to the amorphous structure of the film, thereby limiting its application in high-speed applications.

Deposition of polycrystalline silicon (polysilicon) is a mature, CMOS compatible process that is easy to deposit on a variety of substrates. In addition, it can be easily doped to realize electrically active photonic devices due to its relatively high ($\sim 100 \text{ cm}^2/\text{V}\cdot\text{s}$) [1] electronic carrier mobility. Propagation loss has remained a significant challenge for polysilicon waveguides, which is dominated by scattering and absorption at the polycrystalline grain boundaries. Low loss ($\sim 6.45 \text{ dB/cm}$) polysilicon waveguides, [2, 3] high quality factor ring resonators [4], and high speed electro-optic modulators [5] formed by Solid Phase Crystallization (SPC) of Low Pressure Chemical Vapor Deposition (LPCVD) amorphous silicon have been demonstrated. Compared to direct deposition of LPCVD polysilicon, SPC of LPCVD amorphous silicon yields superior film qualities, such as smoother surfaces to reduce interfacial scattering and larger grains that result in fewer absorbing and scattering boundaries, further lowering the propagation loss [6].

To date, photonic polysilicon research has focused on waveguides and devices in the single mode region with thicknesses of 200-250nm and widths of 300-500nm, where narrower waveguides result in lower loss due to less confinement of light in the polysilicon core, indicating that attenuation is dominated by bulk loss [2]. Indeed, efforts to further reduce the overlap of the optical mode with the waveguide cross section have been made by forming polysilicon waveguides in the same step as the polysilicon transistor gate for electronics, resulting in core geometries of 120nm X 350nm and a propagation loss of 6.2 dB/cm at 1550nm. Unfortunately, little work exists for wider, multimode polysilicon devices. Liao et al have reported that thicker and wider polysilicon waveguides suffer from higher propagation losses due to increased optical confinement[Liao2000]. However, for key photonic components such as multimode interference couplers (MMI) for beam splitting and arrayed waveguide gratings (AWG) for wavelength division multiplexing (WDM), device dimensions can span tens to hundreds of microns in width [7, 8]. Characterizing the loss of polysilicon at such widths is necessary to determine if these devices can be formed without prohibitively high losses.

In this paper, we fabricate polysilicon waveguides of various widths and investigate the propagation loss dependence of these waveguides on the waveguide width and also compare with the same structures on crystalline SOI. We find that as the waveguide width increases, the propagation loss for both polysilicon and crystalline silicon waveguides decreases. At the widest waveguide width of 10 μ m, both polysilicon and crystalline silicon have low loss values of 0.56dB/cm and 0.31dB/cm, respectively, indicating very little bulk absorption occurs in the polysilicon film. To the best of our knowledge, this is the lowest demonstrated loss for polysilicon waveguides to date. Moreover, the first 1x12 polysilicon MMI is presented with an insertion loss of -1.29dB and a uniformity of 1.07dB.

2. Design and Fabrication

We have used the beam propagation method (BPM) from Rsoft to simulate 10 μ m wide waveguides for both crystalline silicon and polysilicon with grain boundaries, which is shown in Figure 2 (a) and (b), respectively. Figure 2(a) shows the 10 μ m wide crystalline silicon waveguide excited by the fundamental mode, which propagates through the waveguide undisturbed. In contrast, a polysilicon waveguide is simulated by adding grain boundaries. The grain boundaries scatter light into higher order modes that are still guided by the wide waveguide. For narrower waveguides, the grain boundaries scatter light into radiative modes, as higher order modes are not guided. Therefore, the number of guided modes in a given waveguide geometry determines the propagation loss due to grain boundary scattering.

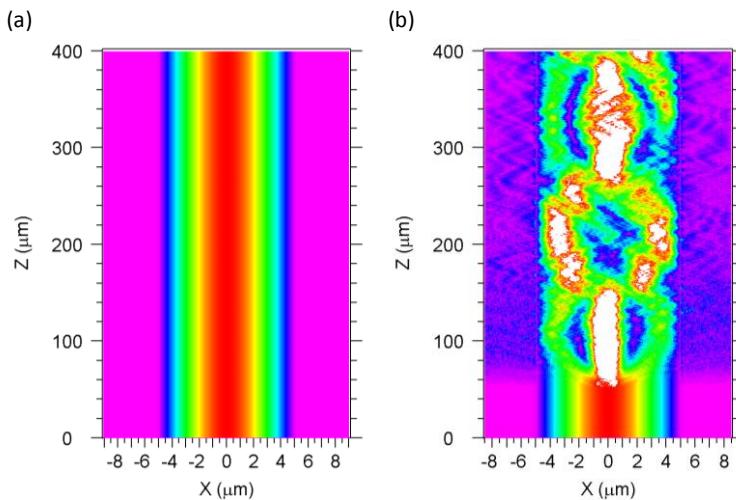


Figure 3-1-Beam Propagation Method simulation of $10\mu\text{m}$ waveguide for (a) crystalline silicon and (b) polysilicon with grain boundaries.

In order to investigate the effect of the waveguide width on the propagation loss of polysilicon waveguides, the waveguide width is varied by using the structure shown in Figure 2. For each waveguide width, the input and output waveguides have the same dimensions to equalize the coupling conditions. We first adiabatically taper all waveguide widths to 500 nm in order to filter out higher order modes and achieve single mode propagation. The waveguide is then adiabatically tapered to the desired waveguide width, which ranges from 400 nm to 10 μm . After 5 mm of propagation, all waveguides are then tapered back to the output waveguide width. The same structures are also fabricated on crystalline silicon as a reference. By having the exact same structure and fabrication process, our results can only arise from the differences between the two materials.

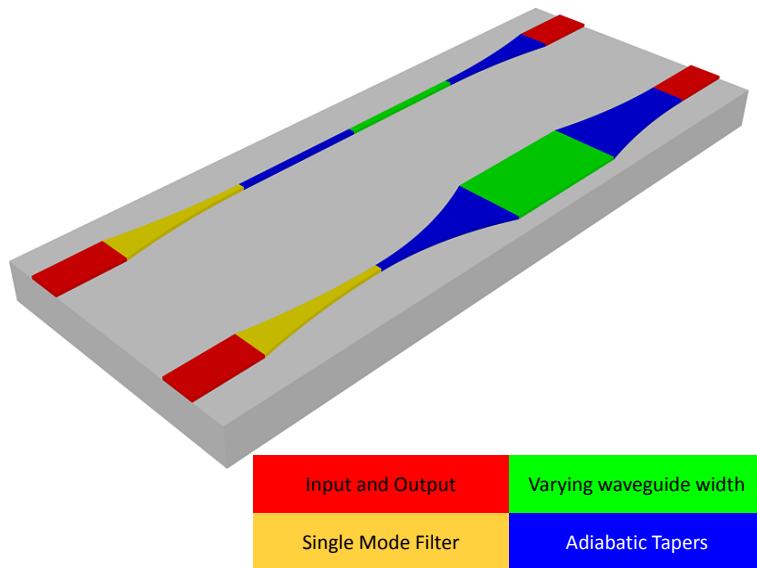


Figure 3-2-Schematic of multimode waveguide structure. Not drawn to scale.

In addition, we also designed a 1×12 Multimode Interference (MMI) optical beam splitter to further demonstrate large multimode polysilicon devices. The length and width of the multimode region are $L_{MMI}=563.4 \mu\text{m}$ and $W_{MMI}=60 \mu\text{m}$ respectively. The input and access waveguides are both $2.6 \mu\text{m}$ wide. To clearly resolve the individual output spots in the near field, a fanout design was used to separate the 12 MMI output channels to $30 \mu\text{m}$. A schematic of the 1×12 MMI can be seen in Figure 3.

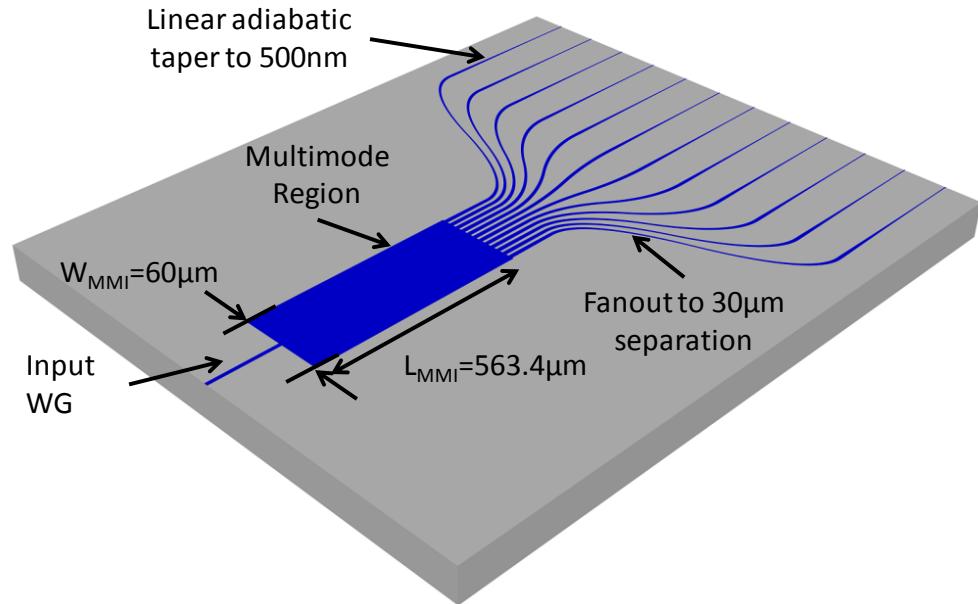


Figure 3-3-Schematic of 1×12 MMI

In our experiment, we thermally oxidize a bare silicon wafer to create $2.0 \mu\text{m}$ of SiO_2 which acts as the BOX layer and is thick enough to prevent optical leakage into the substrate. Afterwards, a 250nm thick layer of amorphous silicon was deposited using Low Pressure Chemical Vapor Deposition (LPCVD) at 550°C . From [Hatalis1998], we find that the deposition rate should be sufficiently high to minimize the number of nucleation sites, which results in increased grain size. Consequently, we use an increased silane gas flow to achieve a deposition rate of $3.3\text{nm}/\text{minute}$. After the amorphous silicon deposition, we briefly dip the wafers in Piranha solution to form a native oxide layer. This thin native oxide layer stabilizes the top surface of the amorphous silicon and prevents increased surface roughness during future anneal treatments[Ibok93]. The wafers are then annealed using a two-step annealing process. The first anneal is a low temperature anneal that is done at $600^\circ\text{C} \text{ N}_2$ for 40 hours, and the purpose of this anneal is for gradual grain nucleation, which results in large grains. The second anneal is a 5 hour 1000°C also in N_2 , and this step is to crystallize the individual polysilicon grains.

In order to estimate our grain size, we use dry oxidation at 900°C for 30 minutes to oxidize the top surface of our polysilicon film. Because polysilicon grains will preferentially oxidize along grain boundaries, we can use Buffered Oxide Etch (BOE) to remove the oxide and then use

Scanning Electron Microscopy (SEM) to visualize our grains. A picture of such an SEM image is shown in Figure 5(a), and we estimate the grain sizes to be \sim 300nm.

A 45nm layer of PECVD SiO₂ is deposited to serve as an etching hard mask. Our waveguides were patterned using a JEOL 6000FS electron-beam lithography system with ZEP520 resist, and etched with HBr/Cl₂ based Reactive Ion Etching (RIE). Afterwards, a 1 μ m thick film of SiO₂ for top cladding was deposited using PECVD. A cross section view of a single mode polysilicon waveguide is shown in Figure 5(b), and a microscope image of the 1x12 MMI is shown in Figure 5(c).

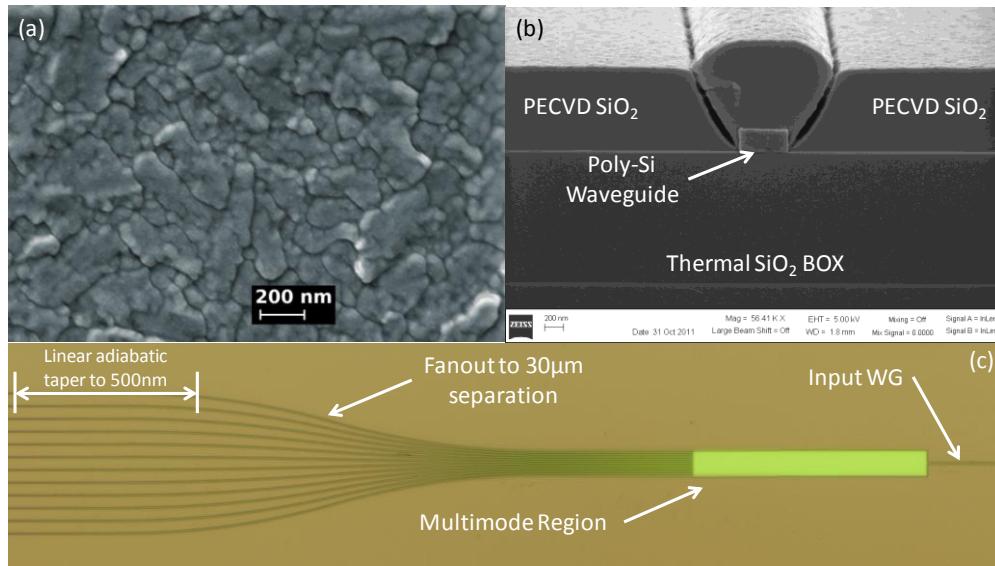


Figure 3-4-(a) Top down SEM image of polysilicon grains after oxidation and BOE, (b) cross sectional SEM of a single mode polysilicon waveguide and (c) microscope image of the completed 1x12 MMI.

3. Results and Analysis

Transverse Electric (TE) polarized light at 1550nm was coupled into and out of the waveguides using lensed fibers with 2.5 μ m mode field diameters, where the input is a polarization maintaining (PM) fiber, and the output is collected with a single mode (SM) fiber. The propagation loss of various waveguide widths for both crystalline and polysilicon are shown below in Figure 5.

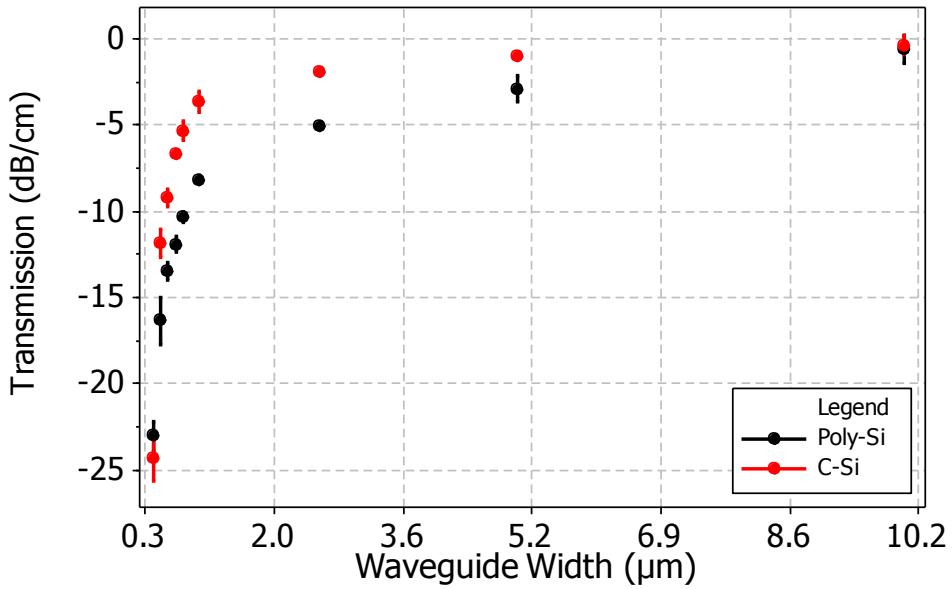


Figure 3-5-Propagation loss of various polysilicon and crystalline silicon waveguide widths.
Standard error bars are given for each data measurement.

The propagation loss decreases for both crystalline silicon and polysilicon as the waveguide width increases. At a waveguide width of 400nm, the propagation losses of crystalline and polysilicon are virtually the same, but as the waveguide width increases, the loss difference between the two also increases. For waveguide widths above 2.5μm, the difference in propagation loss between crystalline and polysilicon decreases until they have nearly identical propagation losses at 10μm. For crystalline silicon, this behavior is well known and is due to decreasing sidewall interaction of the fundamental mode of the waveguide. However, the grain boundaries present in polysilicon cause scattering to either radiation modes or higher order modes depending on whether the waveguide width supports the higher modes. This scattering causes the additional loss between polysilicon and crystalline waveguides of the same width. It is important to note that at a 10μm waveguide width, both polysilicon and crystalline silicon waveguides have the lowest losses of 0.56dB/cm and 0.31dB/cm, respectively. To our knowledge, this value is the lowest propagation loss for a polysilicon waveguide to date. Furthermore, it indicates that there is very little bulk absorption from the polysilicon grain boundaries. This behavior of decreasing propagation loss with increasing waveguide width validates the use of large polysilicon waveguides in photonic integrated circuits.

We also tested our 1x12 MMI to demonstrate a large polysilicon device. As before, TE polarized light at 1550nm was coupled into the 1x12 MMI. Using an IR camera, 12 output spots are imaged from the MMI fanout, which are shown in Figure 6(a). To characterize the performance of this 1x12 MMI, we used lensed fiber to collect each of the 12 output intensities. The performance of an MMI can be described by output uniformity and insertion loss. The uniformity is calculated as $10 \log(I_{\max} / I_{\min})$, where I_{\max} and I_{\min} are the maximum and minimum

output intensities of the MMI, respectively. The insertion loss of the MMI is defined as $-10 \log(\sum I_i / I_{in})$, where I_i is the output intensity of the i^{th} output channel, and I_{in} is the intensity of a straight waveguide with the same dimensions of the MMI input waveguide. For our polysilicon 1x12 MMI, we determine a uniformity of 1.07dB and an insertion loss of -1.29dB. The insertion loss is a negative number because the output intensity of the input waveguide used for normalization is lower than the sum of the MMI output intensities. This is due to the presence of the multimode region of the MMI, which is 60 μ m wide and 563.4 μ m long and has a much lower loss compared to the much narrower input waveguide. We have previously demonstrated a 1x12 MMI on crystalline silicon with comparable performance [10].

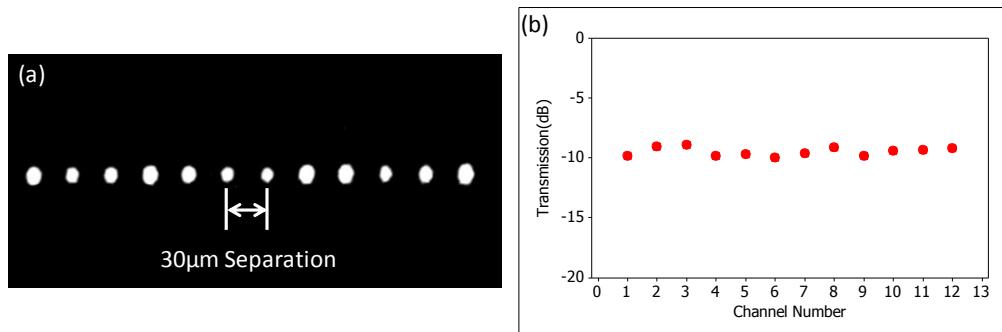


Figure 3-6-(a) IR image of the 12 output spots from 1x12 MMI fanout. (b) Output intensities of the 1x12 polysilicon MMI.

4. Conclusion

We have investigated the feasibility of multimode polysilicon waveguides to demonstrate the suitability of polysilicon as a candidate for multilayer photonic applications. SPC with a maximum temperature of 1000°C is used to create polysilicon on thermal SiO₂. We then measure the propagation losses for various waveguide widths on both polysilicon and crystalline silicon platforms. We find that as the width increases for polysilicon waveguides, the propagation loss decreases similarly to crystalline silicon waveguides. The difference in loss between the two platforms for a given waveguide width is due to the scattering from the polysilicon grain boundaries, which excites higher order modes. Depending on the waveguide width, these modes either propagate as higher order modes or are lost as radiation modes. We also find that at a waveguide width of 10 μ m, the polysilicon propagation loss of 0.56dB/cm is very close to the crystalline silicon propagation loss of 0.31dB/cm, indicating that there is little bulk absorption from the polysilicon. This result validates the use of polysilicon waveguides in photonic integrated circuits. We further demonstrate this with a 1x12 polysilicon MMI that has a low insertion loss of -1.29dB and a high uniformity of 1.07dB. Together, we present the lowest propagation loss for polysilicon waveguides to date of 0.56dB/cm as well as the first 1x12 polysilicon MMI.

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4.0 Vertically Integrated Double-layer On-chip Silicon Membranes for 1-to-12 Waveguide Fanouts

Large on- and off-chip bandwidths required for high performance multi-core structures (~10TB/s by 2015) corresponding to interconnect energy budgets of ~100 fJ/bit will render optical components essential parts of future high performance integrated systems [1-3]. Complementary metal-oxide-semiconductor (CMOS) compatible silicon photonics, which allows for integration of optical components on the same silicon chip with CMOS transistors, is considered one of the solutions to such a high demand for low energy and high bandwidth communications [3, 4]. Since the Luxtera silicon photonic chip in 2002, the number of on-chip photonic components has doubled each year [5, 6]. There is also a “Moore’s law like” trend observed in InP-based photonic integrated circuit (PIC) development since 1988 [7]. However, due to the large sizes of the on-chip photonic components, single layer photonic component counts cannot exceed 1000 and 10,000 in InP and silicon PICs, respectively [8].

Vertical integration of multiple layers of active and passive components can resolve the problem of limited real estate on a single layer [9]. So far, an extra polysilicon layer on top of the crystalline silicon layer has been used for CMOS microelectronics and photonics integration [10, 11]. This scheme may also be used for three-dimensional (3D) photonics integration. However, the optical losses in polysilicon waveguides are dominated by scattering and absorption at the grain boundaries [10], which increase significantly when the waveguide width shrinks to below 200nm [12]. Techniques such as high temperature annealing, special hydrogen plasma passivation steps, and patterning waveguides before the solid-phase crystallization (SPC) of deposited amorphous silicon were shown to reduce the propagation loss [12, 13]. Lowest losses ranging from 7dB/cm to 13dB/cm were reported in polycrystalline silicon waveguides with cross sectional dimensions of approximately 450 x 250 nm [12, 14, 15], and from 1dB/cm to 2dB/cm in crystalline silicon waveguides with similar dimensions [16, 17]. Additionally, if the temperature process is limited to about 600°C, which is compatible with standard CMOS processes, the Q-factor of the ring resonators fabricated on polysilicon layers drops by an order of magnitude [10, 18], indicating even higher losses.

In this paper we demonstrate a 3D photonic integration of self-aligned structures using double-bonded silicon-on-insulator (SOI) wafers by fabricating double-layer 1x12 multimode interference (MMI) couplers on silicon membranes. Using the presented scheme, multi-levels of PICs including waveguide arrays, MxN MMI couplers, and arrayed waveguide gratings (AWGs) can be vertically integrated to significantly increase the on-chip integrated photonic component count.

The schematic of a 1xN MMI coupler is shown in Figure 1(a). We choose the MMI width, $W_{MMI}=60\mu\text{m}$. The MMI length with a 1xN fanout is given as $L_{MMI} = (n_{eff} W_{MMI}^2) / (\lambda_0 N) = 664\mu\text{m}$ [19], where $n_{eff} = 3.43$ (for 1.3μm thick silicon membrane) is the effective refractive index of the transverse electric (TE) fundamental mode of the multimode waveguide, and $\lambda_0 = 1.55\mu\text{m}$ is the free space wavelength. The input and output access waveguide widths, $W_w = 2.5\mu\text{m}$, match the mode sizes of the input/output lensed fibers. Thus, the fiber-waveguide coupling tolerance is enhanced due to the waveguides’ relatively large end-fire cross sections. The schematic of the double-bonded SOI wafer and self-aligned waveguide structure are shown in Figure 1(b). The thicknesses of both silicon layers are $h_1=h_2=1.3\mu\text{m}$, and the two buried oxide (BOX) layers are both 2.0μm thick. The simulated effective index of the fundamental TE and transverse

magnetic (TM) modes in the access waveguides are 3.417 and 3.412, respectively, at $\lambda=1.55\mu\text{m}$. Polarization independent operation is expected due to the small difference between the TE and TM effective indices. We fabricate two self-aligned 1x12 MMI couplers on two vertically stacked silicon membrane layers using one lithography process followed by a single etching step. MMI couplers can be used for efficient on-chip beam splitting [19]. A complete analysis for a symmetrically excited 1xN MMI coupler with uniform output was presented in Ref. [20].

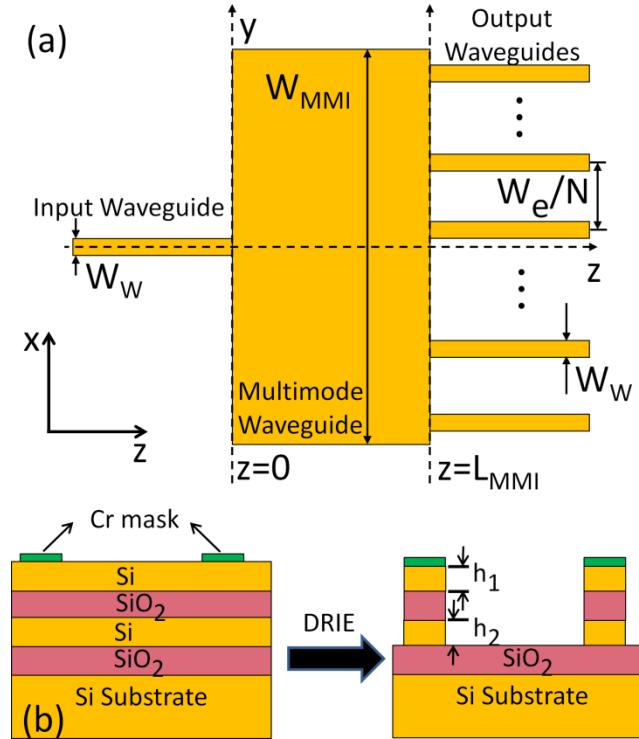


FIG.4-1.(a) The Schematic of a 1xN MMI coupler. (b) The schematic of the double-bonded SOI wafer and self-aligned waveguide structure.

The double-bounded SOI wafers are fabricated using fusion bonding and etch-back [21], and are commercially available from Ultrasil. A 100nm thick chromium etching mask is defined through an e-beam lithography and lift-off process. The pattern is then transferred to both silicon layers using one SF₆/C₄F₈/Ar based Deep Reactive-Ion-Etching (DRIE) step in Plasma-Therm's Versaline system. The DRIE process consists of ~1000 iterations of a two-step polymer deposition/etching cycle. Afterwards, the chromium mask is removed. The sidewall profile control in the DRIE process is the key to the performance of the fabricated devices. Although the Bosch process based DRIE of silicon, which alternates repeatedly between deposition of a polymer passive layer and isotropic plasma etching of silicon, is well developed in industry [22] and the standard recipes are provided by the system manufacturer, it has a very slow etch rate for silicon oxide and is not applicable for etching into double-bonded SOI wafers. In order to achieve a vertical sidewall, several process parameters need to be optimized, including gas composition, bias radio frequency (RF) voltage, inductively coupled plasma (ICP) power, chamber pressure, and step time. A standard recipe (Table I) for etching SOI wafers is used as the base recipe for parameter optimization. Wafer loading and temperature are kept constant during the optimization process.

TABLE 4-I.DRIE base and final parameters for one deposition and etching cycle.

Steps	Gas flow rate (sccm ^a)						Bias voltage (V)	RF power (W)	ICP pressure (mTorr)		Time (s)			
	SF ₆		C ₄ F ₈		Ar				Bas e	Fin al	Bas e	Fin al		
	Bas e	Fin al	Bas e	Fin al	Bas e	Fin al	Bas e	Fin al	Bas e	Fin al	Bas e	Fin al		
Deposition	50	50	125	125	10	10	10	10	160	160	20	20	0.8	0.8
Etching	60	50	40	40	10	10	250	400	120	150	20	20	2	2

^aSCCM denoted standard cubic centimeter per minute at standard temperature and pressure (STP).

By individually optimizing these parameters to achieve vertical sidewalls, we arrive at the final recipe, which is also shown in Table I. We determine that the bias RF voltage has the largest impact on the anisotropy of the sidewall profile. A larger bias RF voltage results in a higher etch rate and yields a more vertical sidewall profile during silicon oxide etching, but it also causes more damage to the polymer layer on the sidewall of the silicon membrane layer. Figure 2(a) shows the cross section of a waveguide etched using our otherwise final recipe with a 450V bias RF voltage. The polymer layer on the sidewall is consumed by the etching step and results in a large undercut to the top silicon layer, leading to significant deviation from the original design. Figure 2(b) shows the cross section of a waveguide etched using the final recipe. The result shows a reduced undercut and a ~80° tapered sidewall profile during the silicon oxide etching. The undercut to the top silicon layer is inevitable due to the required ~40 minute etch time of the BOX layer [23].

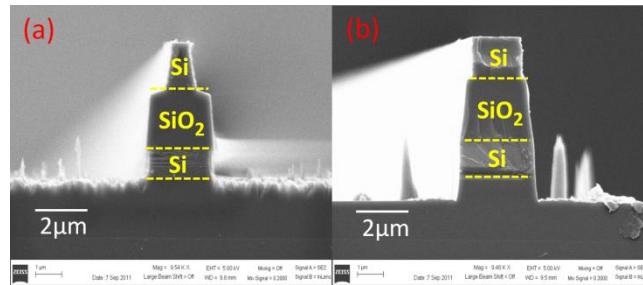


FIG.4-2. SEM images of the waveguide cross section under different etching conditions, (a) a waveguide cross section with large undercut, (b) a waveguide cross section with corrected undercut.

The fabricated MMI access waveguides are 2.0μm and 2.9μm wide on the top and bottom layers, respectively. These access guides also correspond to TE fundamental mode effective refractive indices of 3.410 and 3.419, respectively [Figure 2(b)]. We note that because of the large thicknesses of the silicon layers, the effective index changes negligibly with variations in the waveguide width. Figure 3(a) shows a microscope image of the overall double-layer MMI. Figures 3(b) and 3(c) show the scanning electron microscope (SEM) images of the MMI output region and the output facet, respectively, with their corresponding locations labeled in Figure 3(a).

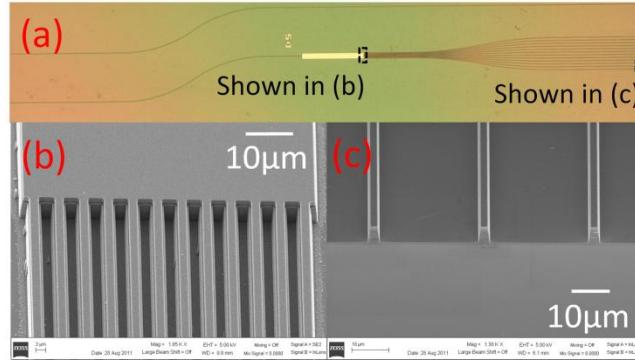


FIG.4-3.(a) Optical microscope image of the double-layer MMI, (b) SEM image of the MMI output region, (c) SEM image of the output waveguide's facet.

A six-axis automated aligner system with a movement precision of 50nmis utilized to couple TE polarized light at a wavelengthof 1550nm from a polarization maintaining lensed fiber (PMF) with a 2.5μm output mode diameter into the silicon waveguide inputs. An infrared (IR) camera connected to a variable objective lens captures the top-down, near-field images of the output facets. In order to visually resolve the 12 output spots, a waveguide fanout design is used to increase the separation of each adjacent channel to 30μm [Figure 3(c)]. In order tovisualize individual layer coupling in our double-layer device, we separate the outputs in the bottom layer from those in the top layer so that the two device layers terminate at two different locations as shown in Figure 4(a). Figures 4(b) and 4(c) illustrate the excitation of top and bottom layer MMI couplers, respectively. These results demonstrate selective coupling to each layer with negligible crosstalk, which in turn is due tothe 2μm thick BOX layer between the two silicon layers. Figure 4(d) illustrates the simultaneous excitation of top and bottom layer MMI couplers.

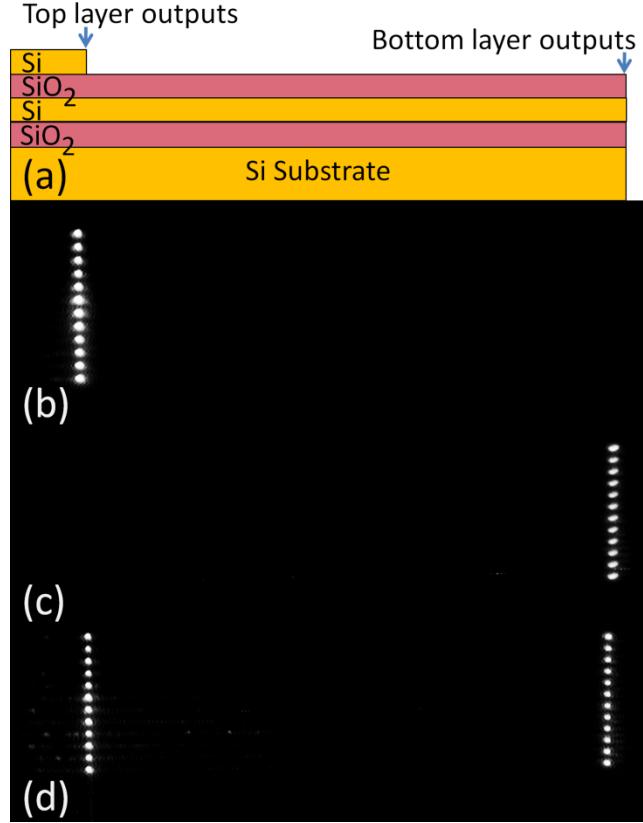


FIG. 4-4.(a) Schematic of separated outputs for the top and bottom layers. (b)IR top-down image of the double-layer MMI coupler with top layer excitation.(c)IR top-down image of the double-layer MMI coupler with bottom layer excitation.(d)IR top-down image of the double-layer MMI coupler with simultaneous excitation to both layers.

We characterize the MMI couplers on both layers by fiber scanning as described in [19]. The chip is cleaved to make measurable facets via fiber for both the top and bottom layers. A single-mode lensed fiber (SMF) is used to scan each output channel to determine the output intensity of each channel and evaluate the performance of the MMI couplers on both layers. The uniformity of an MMI coupler is defined as $10\log(I_{\max}/I_{\min})$, where I_{\max} and I_{\min} are the maximum and minimum intensities of the MMI output channels. The excess loss of an MMI coupler, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{in}]$, where I_m is the intensity of the m^{th} output channel, and I_{in} is the output intensity of a reference waveguide on the same chip with the same cross section dimensions as the MMI access waveguides. Using FIMMPROP's fully vectorialeigenmode decomposition-based complex Film Mode Matching (FMM) solver (with 60 one-dimensional (1D) modes), we calculate the variations of the MMI excess loss and uniformity for both TE and TM polarizations [Figure 5]. Polarization independent operation is expected for a bandwidth larger than 30nm.

The top layer MMI coupler has an excess loss of 0.48dB and a uniformity within 1.1dB, while the bottom layer MMI coupler has an excess loss of 2.9dB and a uniformity within 1.7dB. Since the input waveguide is multimode, the excitation of TE_{0n} and TE_{mn} (m and n are the horizontal and vertical orders of the mode, $m, n > 0$) modes depends on the input field launching condition, and consequently contributes to the excess

loss and output non-uniformity. In our case, the input lensed fiber mode size ($1/e^2$) is $2.5\mu\text{m} \times 2.5\mu\text{m}$, and the input waveguide TE₀₀ mode size is $2.2\mu\text{m} \times 1.1\mu\text{m}$ ($1.6\mu\text{m} \times 1.1\mu\text{m}$) for the bottom (top) layer. With optimized input coupling conditions, input power is mostly coupled to the TE₀₀ mode. The MMI performance is most efficient for the TE₀₀ mode due to it having the highest effective modal index [19]. Under the excitation of the TE₀₀ mode of the input waveguide, TE_{m0} modes will be excited, but TE_{0n} modes will not be excited inside the multimode waveguide region [Figure 1(a)]. By comparing the measured MMI performance metrics of both layers to 1xN MMIs fabricated on a 230nm thick silicon nanomembrane (vertically single mode) [19], we confirm that the higher-order modes (inside the access waveguides) are suppressed with the optimized input coupling condition where most energy is coupled to the TE₀₀ mode. We also find that bottom layer silicon membrane has larger thickness variations than the top layer silicon membrane, which contributes to the differences in device performance for each layer.

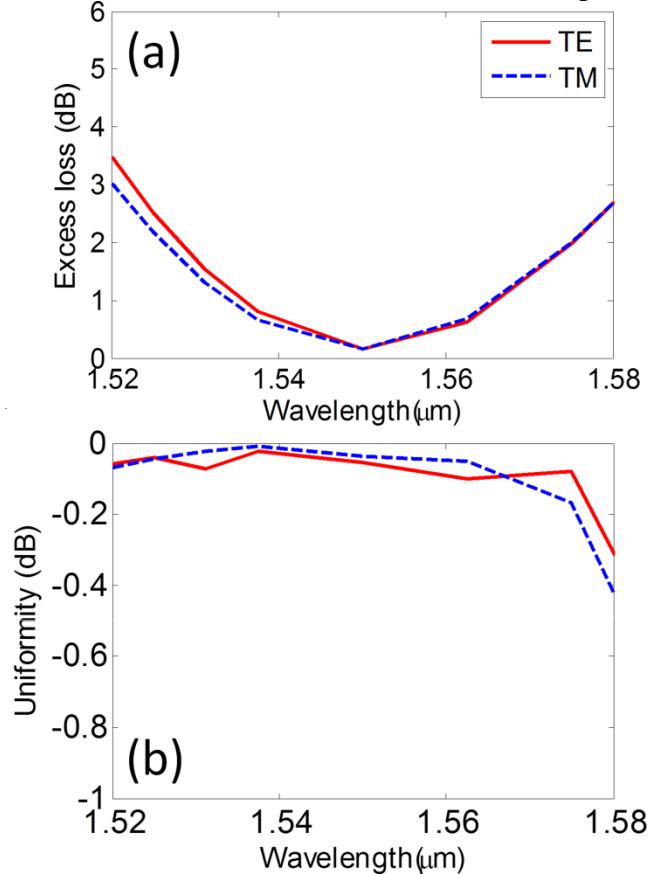


FIG.4-5. Simulated MMI (a) excess loss and (b) uniformity as functions of wavelength for TE and TM polarizations.

In summary, we present vertically integrated, two-layer, low loss, crystalline silicon membranes. We developed a DRIE recipe for fabrication of self-aligned waveguiding structures on double-bounded SOI substrates. The fabricated double-layer MMI couplers show low excess loss [0.48dB (top) and 2.9dB (bottom)] and uniform outputs [within 1.1dB (top) and 1.7dB (bottom) power fluctuation] and can be used for 1-to-many fanouts on different layers in 3D silicon PICs. This approach is a potential solution to the limited silicon real estate problem via vertical integration of integrated photonic devices, such as optical phased arrays (OPAs) [24] and intra- and inter-chip guided wave optical interconnects [25, 26], which require accurate alignment between vertically integrated photonic devices.

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5.0 Double-layer Photonic devices Based on Transfer Printing of Silicon Nanomembrane for Three-dimensional Photonics

Vertical integration of multiple layers of active and passive photonic components can resolve the problem of limited real estate on a single layer silicon photonic integrated circuit (PIC) [1]. So far, deposited polysilicon has been used for photonic integration [2]. This scheme may also be used for 3D photonic integration. However, the lowest reported propagation loss is 6.45dB/cm in polycrystalline silicon waveguides with cross sectional dimensions of approximately 450 x 250nm [3], while being ~1dB/cm in crystalline silicon waveguides with the similar dimensions [4]. Additionally, polysilicon process requires high temperature crystallization anneal (~1100°C), which limit its applications in active photonic devices, such as thermal-optic devices.

In this paper we demonstrate a novel 3D photonic integration scheme using transfer printing of silicon nanomembrane. Transfer printing based assembly techniques represent a potential transformational approach for micro/nanofabrication with far ranging fields of use. At the heart of the method is the use of printing protocols to deposit chemical or physical ‘inks’ in the precise architectures required by devices [5]. We fabricate double-layer 1x12 multimode-interference (MMI) couplers, with bottom layer on silicon-on-insulator (SOI) device layer and top layer on transfer printed silicon nanomembrane.

MMI coupler can be used for efficient on-chip splitting. The design of MMI coupler was described in [6]. We chose the multimode waveguide width, W_{MMI}=60μm and the corresponding multimode waveguide length, L_{MMI}=553.4μm. The input and output access waveguide width was W_w=2.6μm. At this width, the modal phase errors were greatly reduced. The output waveguides were tapered down from 2.6 to 0.5μm for singlemode operation.

Figure 1(a) provides a schematic demonstration of the assembly process for double-layer silicon nanomembrane device platform through transfer printing and patterning steps. The device fabrication started with commercially available SOI from SOITEC with 3μm buried oxide layer (BOX) and 250nm silicon device layer. The fabrication of MMI coupler on the bottom layer using electron beam lithography (EBL) and reactive-ion-etching (RIE) was described in [7]. After etching of the silicon device layer, a silicon dioxide layer of 1.5μm was deposited using plasma-enhanced chemical vapor deposition (PECVD) as the interlayer dielectric between the bottom and top layer. Next, a thin layer (~500nm) of SU8 epoxy adhesive was spin-cast onto the silicon dioxide surface. Partial curing of the adhesive layer via heating and UV flood exposure provided a flat, firm surface for mounting additional nanomembrane as top layer.

Silicon nanomembrane derived from a SOI wafer and measuring 2.05mm x 8.05mm x 230nm were released from the hosts by etching in concentrated (49%) HF and retrieved by a bulk piece of PDMS mounted to a rigid glass backing. Figure 1(b) shows a single silicon nanomembrane on the surface of the stamp after retrieval. The inked PDMS was brought into contact with the adhesive-bearing material stack using a custom alignment system with an integrated heating platform. While in contact, the stamp/nanomembrane/substrate system was heated to ~70°C for 10 minutes to fully cure the adhesive.

After curing, the stamp is slowly (~500μm/s) retracted from the surface, transferring the aligned silicon nanomembrane to the material stack as the top device layer. Figure 1(c) shows the silicon nanomembrane printed onto the multilayer stack. A silicon dioxide layer of 40nm was deposited using electron beam

evaporation as the hard mask for silicon nanomembrane etching. The MMI coupler on the top layer was fabricated using the same EBL and RIE process as the one on the bottom layer.

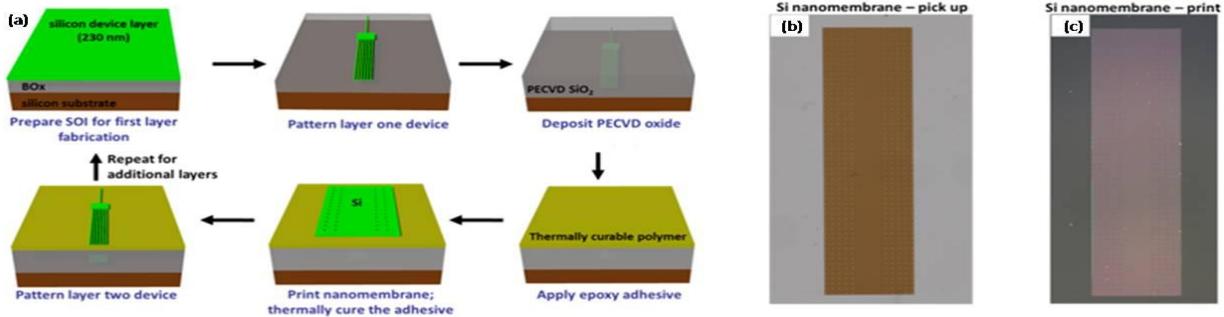


Fig. 5-1 (a) Schematic process flow for assembling double-layer device on silicon nanomembrane. (b) Silicon nanomembrane on the stamp after retrieval. (c) Silicon nanomembrane on the multilayer stack.

Fig 2(a) shows a microscope picture of the fabricated double-layer MMI coupler. Fig 2(b) shows a SEM picture of the cross-section of an output waveguide. An automated aligner system was used to couple TE polarized light at 1550nm from a polarization maintaining lensed fiber (PMF) with a 2.5 μ m output mode diameter into the waveguide inputs. An IR CCD camera connected to a variable objective lens captured the top-down near field images of the output waveguides' facets. A fanout design was used to increase the separation of each output waveguide to 30 μ m for resolve the 12 output intensities for near field imaging. In order to separate the outputs in the bottom layer from those in the top layer, we etched the output waveguides of the top layer to terminate them before where the bottom layer waveguides end as shown in Figure 2(c). Figure 2(d) shows results of simultaneous excitation of MMI couplers on both layers. Efforts are underway to characterize and optimize the device performance, and also assemble large numbers of stacked silicon nanomembranes and active layers into the device platform.

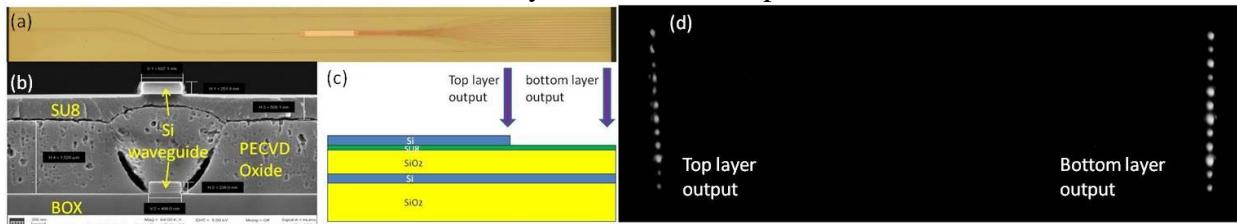


Fig. 5-2 (a) A microscope picture of the fabricated double-layer MMI coupler. (b) A SEM picture of the cross-section of an output waveguide. (c) A schematic showing separated outputs of bottom and top layers. (d) An top-down IR image of the two 1x12 MMI couplers with simultaneous excitation.

In summary, we present a novel vertical integration scheme of large photonic components on multi layers of low loss crystalline silicon nanomembranes by using transfer printing techniques. We developed the patterning and printing process for fabricating double-layer photonic devices and this process can be expanded to large numbers of stacked nanomembrane based photonic devices by repeating the patterning and printing steps. This scheme is a potential solution to the limited silicon real estate for vertical integration of integrated photonic devices, and also serves as platform for novel forms of integrated optical devices.

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6.0 CMOS Compatible High Efficiency Subwavelength Grating Couplers for Silicon Integrated Photonics

Silicon photonics has been considered a promising platform for high density integration of optoelectronic devices.^{1,2} The high index contrast between silicon and its cladding materials (air, silicon dioxide, etc.) allows for the fabrication of submicron structures such as single mode waveguides, resonators, photonic crystals, etc. However, coupling light into and out of these devices through fiber butt coupling suffers from high losses induced by the large mode and effective index mismatches between fiber and strip waveguides with submicron cross sections. The reported efficient coupling schemes include end-fire coupling and off-surface coupling³. The inverse taper, proposed in 2002⁴, has been proved to be an effective solution for end-fire coupling. The highest coupling efficiency demonstrated so far is ~0.5 dB for transverse electric (TE) polarization⁵. The strip waveguide tip must be sufficiently narrow (e.g. 30 nm⁵) to stimulate a delocalized mode. As a result, the height-to-width aspect ratio of the tip is so high that the lithography becomes challenging resulting in a low yield. Furthermore, the resulting mode spot size is still much smaller than that of a single mode fiber, and a lensed fiber is needed to further ameliorate mode matching^{6,7}. In many cases, the chip needs to be diced and polished so that the distance from the nanotaper tip to the chip edge becomes ~3 μm or less⁷. These crucial requirements limit the application of inverse tapers. To overcome these limitations, a subwavelength edge coupler was proposed⁸, and a 0.9 dB coupling efficiency was demonstrated experimentally⁹. The taper width increases to 300 nm, and there is no need for high precision termination at the cleaved chip edge. However, a lensed fiber is still necessary. An alternative solution for achieving high fiber-to-chip coupling efficiencies is the use of a grating coupler (GC)¹⁰⁻¹². Initial efforts in 2006 exhibited a coupling efficiency of 37% and a 1 dB bandwidth of 40 nm¹⁰. The grating required two etches, one of which is a 70 nm shallow etch¹⁰. Subsequently, the addition of an epitaxial silicon overlay enhanced emission directionality to the fiber, thereby increasing the efficiency to 55%¹². The fabrication process contained as many as eight steps, including two etches and an epitaxial growth. The directionality may be further improved using a bottom reflector^{10,13}, but fabrication complexity would significantly increase as well. Using the lag effect of reactive ion etching (RIE), a 64% coupling efficiency was also recently demonstrated¹¹, but the fabrication also involved two etches.

Thus, experimentally demonstrated GCs usually demand complex fabrication processes. Despite these steps, the coupling efficiency leaves room for improvement. Ideally, a GC would be patterned and through-etched in the same step as part of the photonic circuits while yielding a comparable coupling efficiency. However, through-etched air trenches make the grating's index contrast very high. As a result, the Fresnel reflection is prohibitively high, and the coupling efficiency becomes very limited. Efforts have been made in recent years to address this issue. For example, an apodized through-etched GC achieved 35% coupling efficiency with a 1 dB bandwidth of 47 nm at 1536 nm¹⁴. However, index matching oil was needed for this design. One elegant approach is to fill air trenches with a higher index material, but such a solution may not always be available. Fortunately, artificial materials with engineered indices of refraction can also meet these requirements. For example, by using a photonic crystal structure, a 42% peak coupling efficiency was obtained with a 1 dB bandwidth of 47 nm³. Another interesting class of such artificial materials is the subwavelength nanostructure (SWN). Using SWN as a low index material was proposed in 2009¹⁵. A coupling efficiency of 43% (3.7dB) has been reported for TM polarized light around 1550 nm¹⁶. Although promising results have been demonstrated for

TM polarization, few reports have been made about TE polarized fiber-to-chip grating couplers at telecommunications wavelengths on a silicon-on-insulator (SOI) platform¹⁷.

In this letter, we engineer the refractive index of a SWN and demonstrate a TE polarized GC achieving a 59% coupling efficiency at 1551.6 nm. The 3 dB bandwidth is 60 nm. The efficiency increases 1.73 times (from 34% to 59%), and the bandwidth increases 1.5 times (from 40 nm to 60 nm) compared to the previously reported TE polarized SWG on SOI¹⁷. From the manufacturing point of view, the grating can be patterned along with other photonic components through the same lithography and etching process, which significantly reduces the fabrication complexity and also enables integration on other platforms, e.g. flexible photonic components¹⁸.

The subwavelength grating (SWG) proposed in this letter is based on a SOI comprising of a 250 nm silicon device layer and a 1 μ m buried oxide (BOX) layer. The grating is formed by periodically replacing parts of the silicon layer ($n_{si}=3.476$) with SWN, as shown in Fig. 1a. Optimization of the SWG with 3D finite-difference-time-domain (FDTD) is not possible because its simulation time is prohibitively long¹⁶. In this letter, an alternative model is utilized. According to effective medium theory (EMT)¹⁹, a composite medium comprising two different materials interleaved at the subwavelength scale can be approximated as a homogenous medium with an effective refractive index between these two materials. Therefore, the SWG is equivalent to the conventional GC shown in Fig. 1b. The subwavelength region is regarded as a homogeneous material with an effective index n_{sub} ¹⁵. The uniform material is then replaced with a SWN, as shown in Fig. 1c³. To optimize the grating design, a 2D simulation package CAMFR, which is based on the eigenmode expansion technique²⁰, is utilized to search for an optimal combination of grating period Λ_G and n_{sub} giving the highest coupling efficiency to air through the SWG. The duty cycle of the grating is optimized to be 50%, and 25 periods are employed. The grating region is 10 μ m wide and 17.1 μ m long. These dimensions match well with the mode size of a single mode fiber³. An exhaustive parameter sweep shows that the maximum coupling efficiency to air is 72% with an emitting angle of 9.4° when $\Lambda_G=0.685 \mu\text{m}$ and $n_{sub}=2.45$, as indicated in Fig. 2a. The corresponding coupling efficiency to air versus wavelength is shown in Fig. 2b (red curve). To verify the design, 2D FDTD simulations of the grating are also performed, and its results match with those obtained by CAMFR with a discrepancy within 2%. The coupling efficiency to a fiber, shown by the blue curve in Fig. 2b, is evaluated by calculating the overlap integral with the Gaussian mode in a single mode fiber. Since the width of the grating is much larger than its height, decoupled 3D modes can be established in the y and z directions¹⁵. Since the y dependent overlap integral is close to 1²¹, the overlap integral can be simplified to an integration along the z direction. The reflection back into the waveguide is around 3.8% at the wavelength of 1550 nm, as shown by the black curve in Fig. 2b. The design is used for both input and output couplings. The 2D FDTD shows that the difference between input and output coupling efficiency is negligible.

Theoretically, any SWN (e.g. photonic crystals) with an effective refractive index of 2.45 may be used to “fill” the low index regions of a periodic structure, which is a grating in our case. However, as indicated in Fig. 2a, the coupling efficiency heavily relies on n_{sub} , so a precise control of n_{sub} is crucial for achieving high coupling efficiency. In this letter, a thoroughly investigated 1D stratified structure is chosen so that the refractive index of the SWN can be precisely controlled²². As shown in Fig. 1c, silicon and air slices are periodically laminated along the y direction. The guided wave propagation direction is parallel to the layers (z direction) and

the electric field is perpendicular to the layers (y direction). In this configuration the refractive indices of SWN for TE and TM can be calculated through Eqs. (1) and (2) that are shown below²²:

$$\text{TE: } \frac{\sqrt{n_{si}^2 - n_{TE}^2}}{n_{si}^2} \tan\left(\frac{\pi\sqrt{n_{si}^2 - n_{TE}^2} (\Lambda_{sub} - W_{sub})}{\lambda}\right) = -\frac{\sqrt{n_{hole}^2 - n_{TE}^2}}{n_{hole}^2} \tan\left(\frac{\pi\sqrt{n_{hole}^2 - n_{TE}^2} W_{sub}}{\lambda}\right)$$

(1)

$$\text{TM: } \sqrt{n_{si}^2 - n_{TM}^2} \tan\left(\frac{\pi\sqrt{n_{si}^2 - n_{TM}^2} (\Lambda_{sub} - W_{sub})}{\lambda}\right) = -\sqrt{n_{hole}^2 - n_{TM}^2} \tan\left(\frac{\pi\sqrt{n_{hole}^2 - n_{TM}^2} W_{sub}}{\lambda}\right)$$

(2)

Where n_{TE} and n_{TM} are the refractive indices of SWN for TE and TM polarizations, respectively. n_{si} and n_{hole} are the refractive indices of the silicon and the material in the holes, respectively. In our design, the holes are filled with air ($n_{hole}=1$). Λ_{sub} is the period of the SWN, and w_{sub} is the width of the rectangular air holes. The filling factor of the SWN is defined as $f_{sub}=W_{sub}/\Lambda_{sub}$. As the transcendental Eq. (1) and Eq. (2) do not have explicit analytical solution, polynomial expansion is exploited to approximate the tangent function. The n_{sub} versus f_{sub} based on zeroth-order and second-order approximations are illustrated in Fig. 2c. The zeroth-order approximations are accurate only under the condition that along any arbitrary direction, the change in the electromagnetic field within a distance of Λ_{sub} is sufficiently small²². The condition can be formulated as $2\pi n_{eff} \Lambda_{sub} / \lambda \ll 1$. Here, n_{eff} is the mode effective index in the silicon slab waveguide with 250 nm thickness. For TE polarization, the corresponding f_{sub} for $n_{sub}=2.45$ is ~ 0.09 according to the first-order approximation. The smallest w_{sub} that can be fabricated is ~ 40 nm. Thus, Λ_{sub} becomes close to the wavelength inside the slab waveguide. The zeroth-order approximations, therefore, are no longer applicable²³. Including second-order expansion terms can improve the accuracy of the approximation as long as the permittivity of one material is not vastly different from the other^{16,17,22}. Fig. 2c confirms that the first-order approximation underestimates the refractive index by 0.33 when the filling factor f_{sub} is 20%. Thus, the second-order approximation is used in this letter. Considering fabrication yield and repeatability limitations, the trench width is fixed to 80 nm with a corresponding Λ_{sub} of 388 nm.

The designed GC is fabricated using electron beam lithography (EBL) and RIE. The top view and the cross view scanning electron microscopy (SEM) images of the fabricated grating are shown in Fig. 3. A magnified view of the air trenches is shown in the inset of Fig. 3a. The GC is characterized by measuring the fiber-to-waveguide-to-fiber insertion loss. The measurement setup is shown in Fig. 4a. The input and output fibers are mounted on two 10° wedges, which are in turn mounted on rotating stages. The tilt angle can be adjusted from 0° ~ 20°. For this design, both the input and output fibers are tilted $\sim 9.4^\circ$ from normal incidence. The fiber positions are controlled by two xyz stages. A camera is mounted at a 45° angle to visually aid alignment. The input fiber is a polarization maintaining fiber (PMF), and the polarization is controlled via a polarization controller (PC). Light is coupled into an 8 mm long, 2.5 μm wide waveguide via a pair of grating couplers. Since the fundamental mode contains most of the power, the existence of higher order modes has negligible effects on the testing results. A pair of linear waveguide tapers, each with a length of 500 μm , is utilized to bridge the 10 μm wide grating region to the

waveguide. The coupling efficiency is extracted assuming equal coupling efficiencies for both gratings. The transmission spectrum, as shown in Fig. 4b, is measured with a broad band amplified spontaneous emission (ASE) source. The peak efficiency is measured to be 59% (-2.29 dB). The peak wavelength shifts to 1551.6 nm possibly due to fabrication errors. The 1 dB and 3 dB bandwidths are 32 nm and 60 nm, respectively. The Fabry-Perot fringes near the peak wavelength are ~0.3 dB in magnitude, indicating low back reflection. It is much smaller than conventional through-etched GC due to the SWN not only reducing the Fresnel reflection and also functioning as a destructive interference enhancer to reduce the reflection at the interface of the grating and free space¹⁶. The efficiency increases 1.73 times (from 34% to 59%), and the bandwidth increases 1.5 times (from 40 nm to 60 nm) compared to the previously reported TE polarized SWG on SOI¹⁷. The performance enhancement is due to the fact that the refractive index of the SWN is more precisely controlled compared to the previously reported GC¹⁷. The bandwidth can be further extended through increasing the tilt angle²⁴. In this manner, back reflections may also be further suppressed¹⁶. The high efficiency of the grating also benefits from destructive interference in the BOX layer. Due to the interference effects from the downward diffracted light beam, the waveguide to free space coupling efficiency has a strong periodic dependence on the BOX thickness. The coupling efficiency could vary by as much as 30%, as illustrated in the inset of Fig. 4b. The commercially available 1 μ m BOX is close to the optimum thickness yielding the highest upward power efficiency. For comparison, the same design is also fabricated on an SOI with a 3 μ m BOX, which is close to the lowest point in the power efficiency curve shown in the inset of Fig. 4b. For the 3 μ m BOX SWG, the measured peak efficiency is 42.8% (-3.69 dB) at 1550.7 nm with 1 dB and 3 dB bandwidths of 28 nm and 52 nm, respectively. As expected, the performance is worse than that of 1 μ m BOX but is still acceptable compared to recently reported gratings. To verify fabrication repeatability, 32 grating pairs, with 16 pairs on each of the 1 μ m and the 3 μ m BOX chips are fabricated. The measured peak wavelengths and coupling efficiencies are shown in Fig. 4c. Peak wavelength and power vary by 1.1 nm and 0.38 dB for 3 μ m BOX devices and 2.2 nm and 0.52 dB for 1 μ m BOX devices, demonstrating acceptable consistency.

In conclusion, we proposed and demonstrated a through etched SWG coupler, which can be patterned together with photonic components without additional patterning steps. The grating achieves a peak coupling efficiency of 59% with a 3 dB bandwidth of 60 nm on a 1 μ m BOX SOI. This performance is competitive to gratings requiring at least one extra etching step. Testing results of 32 grating pairs show very consistent performance.

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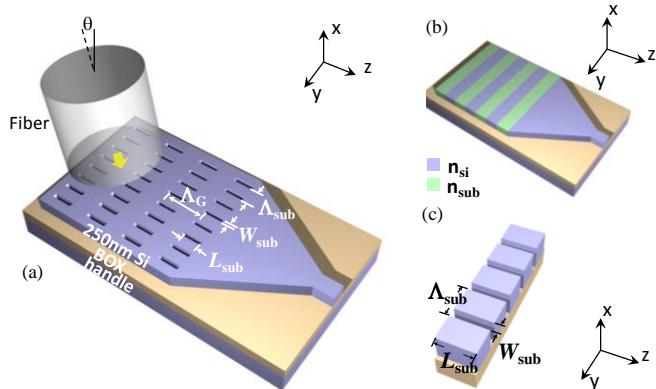


FIG. 6-1 (a) Schematic of the proposed SWG. (b) The equivalent conventional GC. The trenches are filled with SWN of refractive index n_{sub} . (c) Schematic of the SWN. The refractive index of the material can be controlled by tuning the width W_{sub} of the rectangular air hole and the period Λ_{sub} of the subwavelength structure

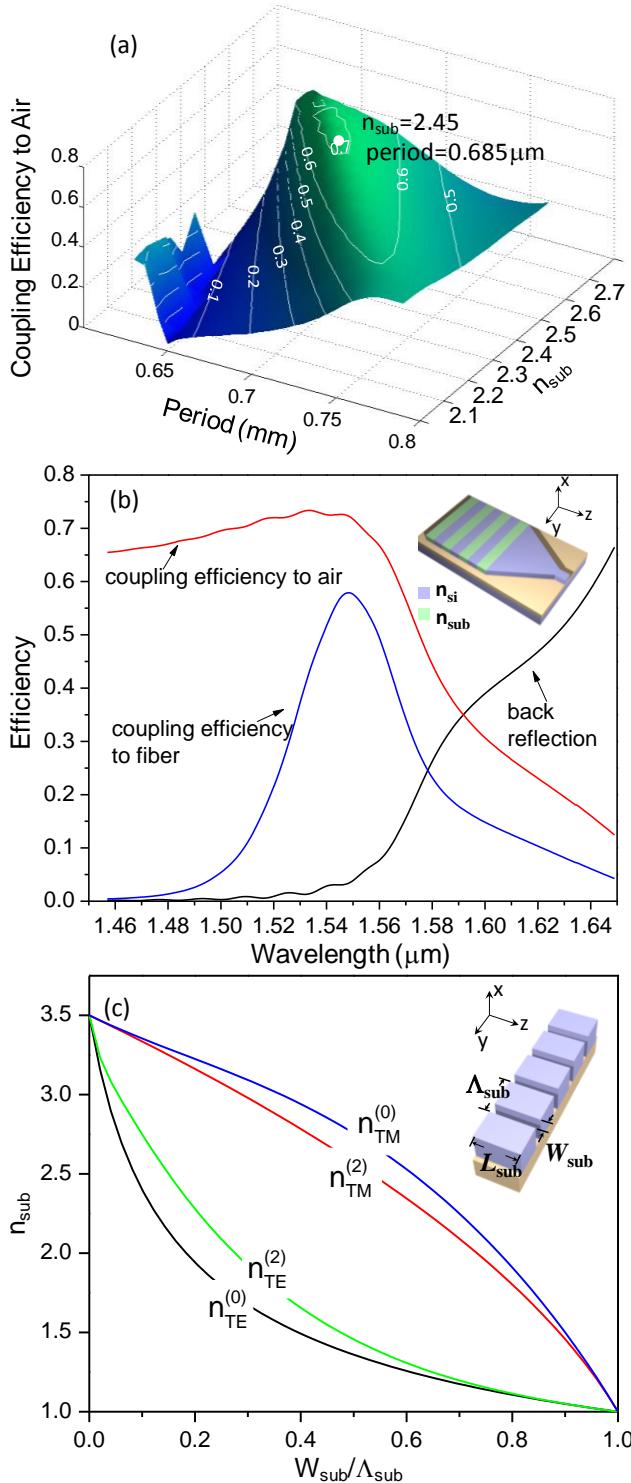


Fig. 6-2. (a) Coupling efficiency to air as a function of grating period Λ_G and the effective refractive index n_{sub} of the subwavelength structure. The highest coupling efficiency to air (white dot) is obtained when Λ_G is $0.685\text{ }\mu\text{m}$ and n_{sub} is 2.45. (b) Coupling efficiency to air (red), Coupling efficiency to fiber (blue), and back reflection (black) from the simplified structure shown in the inset. (c) Refractive index of the SWN for different filling factors, calculated by EMT with zeroth-order and second-order approximations when Λ_{sub} is 300 nm .

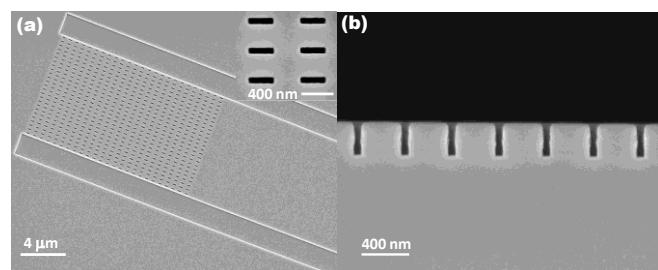


FIG. 6-3. (a) SEM images of the fabricated GC. Inset: the magnified view of the air trenches. (b) the cross section of the rectangular air holes

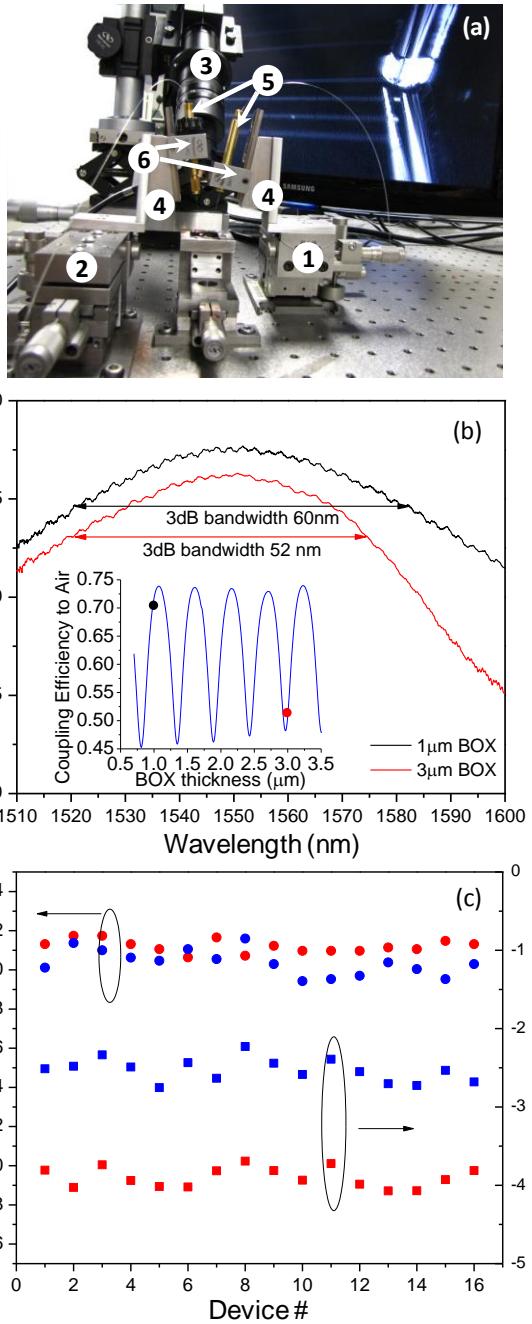


FIG.6- 4 (a) Testing set up. 1. tilting stage; 2. xyz stage; 3. 45° tilted camera; 4. 10° wedges; 5. fiber chuck; 6. chuck holder; (b) The measured transmission of the grating fabricated on the SOI with $1\mu\text{m}$ BOX (black) and $3\mu\text{m}$ BOX (red). Inset: Upward power efficiency vs. BOX thickness. (c) The peak wavelengths (dots) and the coupling losses (squares) of the fabricated 32 grating pairs on SOI with $1\mu\text{m}$ (blue) and $3\mu\text{m}$ (red) BOXs.

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7.0 On-chip spot size converter for fiber to chip coupling

In many photonic devices, interface problems are normally the most difficult ones to address. A good example of this issue is the strip waveguide-photon crystal waveguide interface. Without a properly designed interface, large mode profile mismatch and group index mismatch will cause strong back reflection and scattering, resulting in a very high coupling loss. In order for a silicon photonic integrated circuit to be implemented in any commercial optical communication or sensor systems, it is necessary to have good coupling efficiency to a fiber. However, there exists a strong optical mode profile mismatch between a silicon waveguide and an optical fiber. Because of the high index contrast in a silicon waveguide, the cross section for such a waveguide is only 230nm by 500nm. By contrast, a single mode optical fiber has a diameter around 9 microns. As a result, this geometrical mismatch causes strong optical mode mismatch, which are shown in Figure 7 - 1. At a fiber-silicon waveguide interface, the small mode overlap between the guided modes makes the optical coupling from an optical fiber to a silicon waveguide very inefficient.

To address this issue, many approaches was proposed and implemented. These include grating couplers¹⁻⁴ and on-chip spot size converters based on inverted tapers⁵⁻¹⁰. It has been reported that 31% coupling efficiency is achieved using grating coupler¹. Adding a gold bottom mirror to the SOI substrate has improved the coupling efficiency to 69%³. Non-uniform grating fabricated using the lag effect in a etch process also shows 64% efficiency⁴. To increase the tolerance of etch process control, a photonic crystal grating using fully etched grating was also demonstrated with 42% peak coupling efficiency.

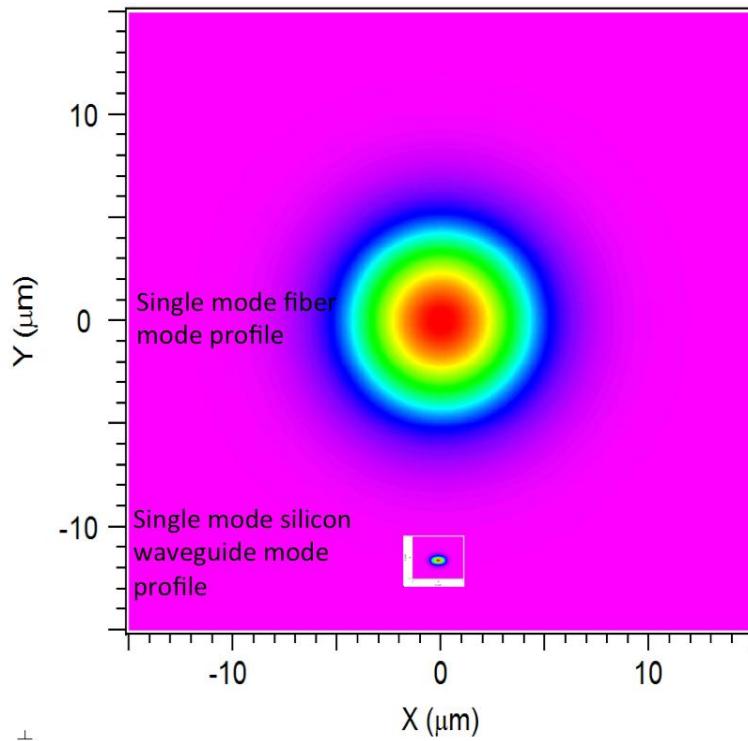


Figure 7 - 1. Optical mode profiles for a single mode fiber and a single mode silicon waveguide with 230nm

Although optical coupling are much more efficient with grating couplers, good coupling efficiency is polarization and wavelength dependent. By contrast, an on-chip spot size converter does not suffer from these restrictions. A schematic of an on-chip spot size converter is shown in Figure 7 - 2. Such structure utilizes an inversely tapered silicon waveguide and a low index waveguide on top of silicon waveguide to significantly reduce the confinement and increase the mode size^{6,7,9,10} when the width of the silicon waveguide is reduced. This results in a loosely confined mode with a mode size that matches that of a optical fiber. In our study, we choose SU-8 photoresist to form the low index waveguide due to several reasons. First, SU-8 can be pattern easily with photolithography or electron-beam lithography. Second, SU-8 is highly transparent near 1550nm. Third, SU-8 is mechanically and chemically stable under room temperature after it is cross-linked. Finally, the refractive index (n) of SU-8 is 1.575 at 1550nm, which can form a waveguide with air cladding ($n=1$). It can also serve as cladding material for silicon waveguide ($n=3.47$). These characteristics make SU-8 a very good material for a proof of concept experiment.

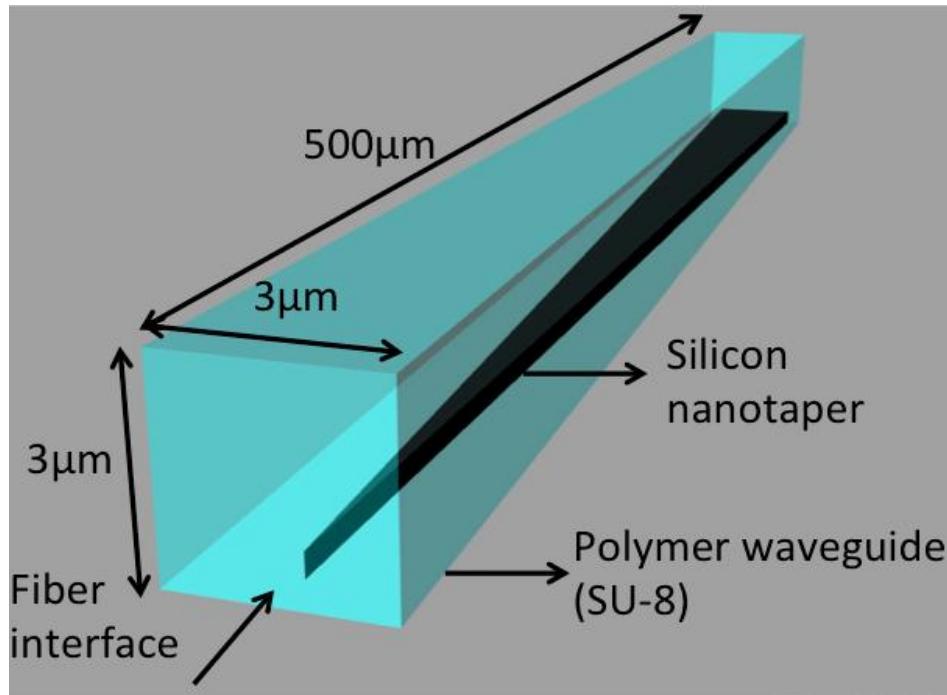


Figure 7 - 2. Schematic of the on-chip spot size converter made of a silicon nanotaper ($n=3.47$) and a polymer waveguide ($n=1.575$)

7.1 Design of on-chip spot size converter

A mode conversion process in the spot size converter is illustrated in Figure 7 - 3. At the end of a silicon nanotaper with 50nm silicon width, the TE guided mode is mostly confined in SU-8 waveguide region as shown in Figure 7 - 3 (a). The dimension of the SU-8 waveguide is chosen to be 3 μ m by 3 μ m to mode match with a lensed fiber. At the fiber interface, input light from a fiber will excite a waveguide mode in the SU-8 waveguide with small optical loss. Moving away from the fiber interface, the width of the silicon nanotaper increases gradually from 50nm to 500nm within 500 μ m distance. As the width of the silicon nanotaper increases, the guided mode

will gradually couple to the high index silicon at the bottom of the SU-8 waveguide. When the width of the silicon taper reaches 500nm, light becomes mostly confined in the silicon waveguide. As a result, the SU-8 structure no longer works as a waveguide; instead, it becomes a cladding layer for the single mode silicon waveguide. This phenomenon is shown in a series of pictures from Figure 7 - 3 (a) to (f).

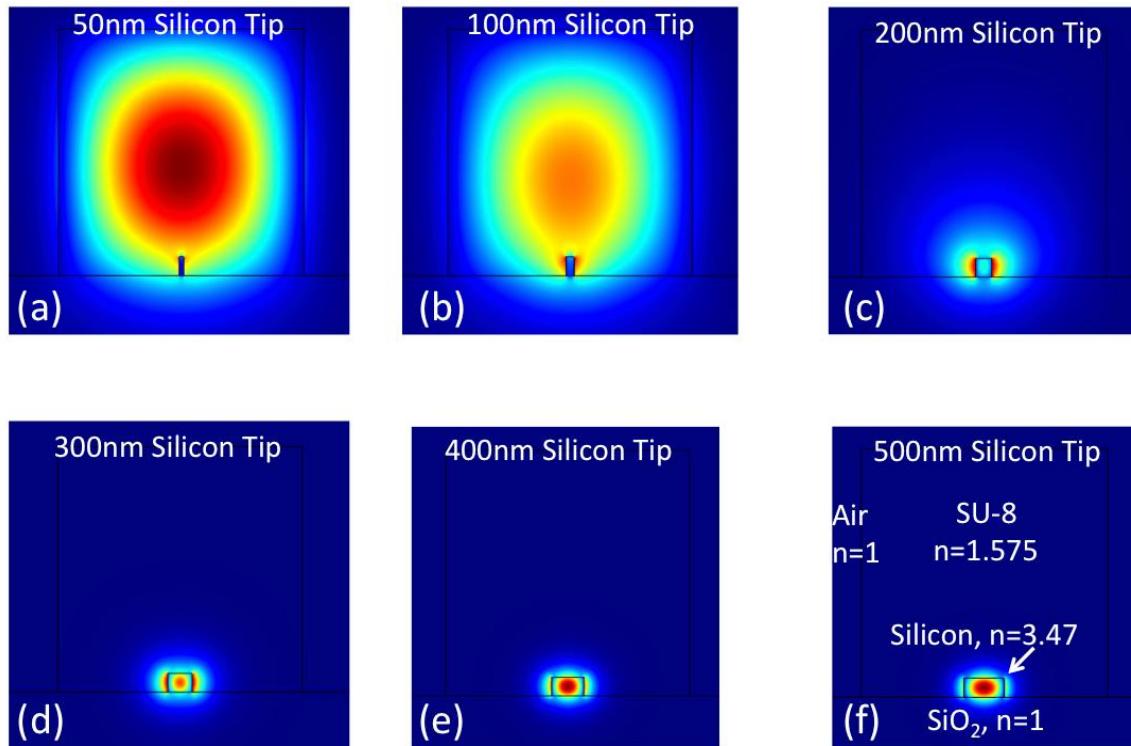


Figure 7 - 3. Transverse electric (TE) optical mode profiles for silicon nanotapers at 1550nm wavelength with (a) 50nm to (f) 500nm width. The height of the silicon nanotaper is determined by the thickness of the silicon slab (230nm).

7.2 Fabrication of the on-chip spot size converter

The fabrication of the silicon nanotaper shares identical processing steps with slotted photonic crystal waveguide modulators as described in Chapter 5. The SU-8 polymer waveguide can be made with a standard photolithography using EVG620 mask aligner in microelectronic research center cleanroom.

The first step is to spin SU-8 2005 on SOI chip with 8000rpm for one minute, followed by a soft bake at 95 degree C on a hotplate for 2minutes. This creates a SU-8 film with $\sim 4.7\mu\text{m}$ thickness. The second step is to UV expose the SU-8 film for 6.5 seconds on the EVG620 mask aligner, followed by a post exposure bake on a hotplate at 95 degree C for three minutes. The exposed SU-8 will start to cross-link after 30~40 sec of baking and the pattern will show up accordingly. After the chip is cooled down to room temperature, it should be developed for one minute in SU-8 developer followed by one-minute IPA rinse. Finally, the chip is hard baked at 160 degree C

for 10 minutes for the SU-8 resist to cross-link. After the SU-8 is cross-linked, it becomes a permanent structure that works as an optical waveguide.

7.3 Measurement and discussion

Measurements were first performed on SU-8 waveguides fabricated on SOI chip with top silicon layer removed. The testing procedure and equipment are identical to Chapter 3. The same SU-8 waveguide before and after baking are both tested for comparison. Measurement results and the microscope pictures are shown in Figure 7 - 4.

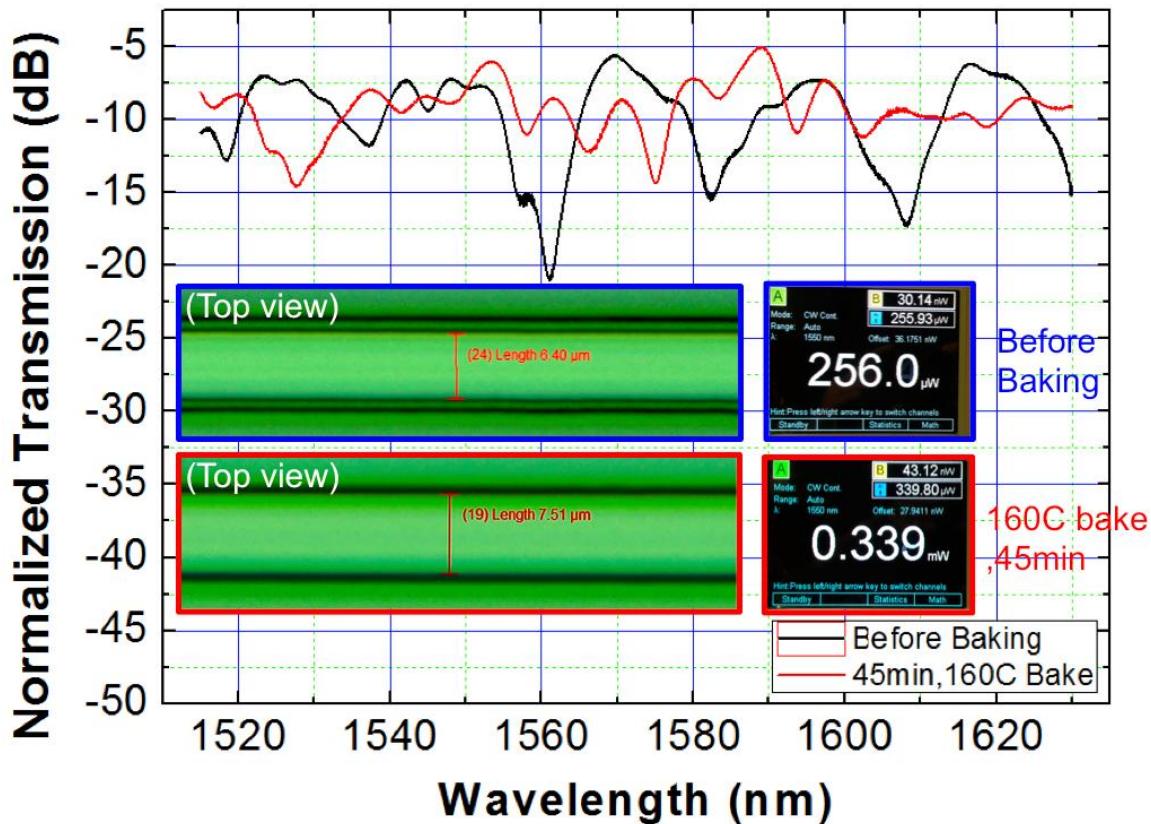


Figure 7 - 4. Measurement result of the transmission spectra for the same SU-8 waveguide before and after baking. The insets show the top view of SU-8 waveguides before and after baking. The insets on the right shows the screen shots of the power meter that display the total power collected at the output fiber.

The measurement results show that it is possible to achieve a broadband coupling with moderate insertion loss. The lowest insertion loss is around 5dB at 1590nm. The fluctuations in the transmission spectrum are mainly due to Fabry-Perot effect at a fiber and chip facet interface. Note that the SU-8 waveguide geometry is not yet optimized, and it is 7.5 μ m wide and 4.3 μ m high. This non-optimized geometry causes optical mode mismatch at the SU-8 and fiber interface and increases insertion loss. With further process optimization, it is expected to get lower insertion loss performance.

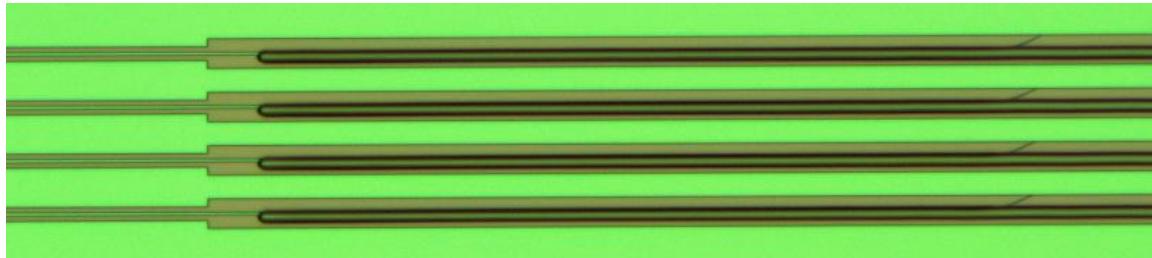
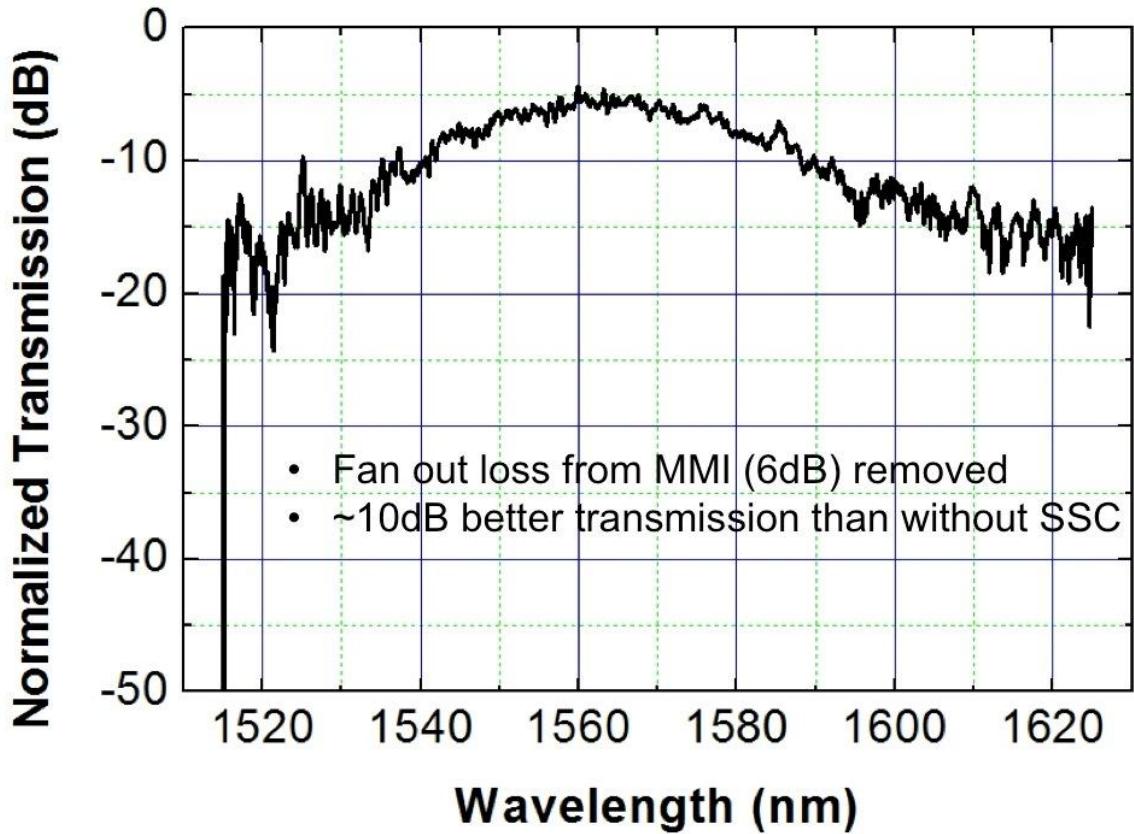


Figure 7 - 5. Transmission spectrum of a silicon strip waveguide from one of the four channels of a 1x4 MMI. Spot size converters are included in both input and output.

The testing result of using spot size converters on all four channels of the TTD module is shown in Figure 7 - 5, and the microscope picture of the output is shown in the bottom panel. The result shows a minimum insertion loss around 5dB, which includes the coupling loss between fiber and SU-8 waveguide and propagation loss in 8mm long silicon waveguide. Compare to the best result in the literature, which has 1dB/facet coupling loss, our result shows higher insertion loss. This is mainly due to the misalignment of SU-8 waveguide on top of silicon nanotaper and the bending of silicon nanotaper tip that make the mode conversion process in the silicon nanotaper region less efficient. The bending of silicon nanotaper tip issue is caused by the bending of e-beam resist pattern during development process, and it is transferred to the silicon layer during subsequent etching processes. The silicon nanotaper tip has 100nm tip width and the resist thickness is around 300nm. During development process, the tip structure with high aspect ratio formed on e-beam resist tends to collapse. Therefore, it is often necessary to reduce the pattern

aspect ratio at the tip region of silicon nanotaper. This problem can be solved by using diluted ZEP520A, which can give 131nm-thick resist layer and significantly reduce the aspect ratio at the silicon nanotaper tip. With further process optimization to eliminate the bending of silicon nanotaper, we expect further reduction of insertion loss using the spot size converter we designed.

7.4 Conclusion

In conclusion, we have shown the design and experimental results as a proof of concept for a low loss and broadband on-chip spot size converter that can significantly reduce the insertion loss between a optical fiber and a silicon photonic chip. This structure will create a better interface between a fiber and a silicon photonic chip, and help drive the implementation of silicon photonics technology in areas such as optical communications and sensors.

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8.0 Coupling Loss Minimization of Slow Light Slotted Photonic Crystal Waveguides Using Mode Matching with Continuous Group Index Perturbation

Slotted photonic crystal waveguides (Slotted PCWs) offer a unique platform that merges the best properties of slot waveguides and photonic crystal waveguides (PCW): strong optical confinement in slot waveguides¹⁻⁴ and slow light enhanced light-matter interaction in PCWs⁵⁻⁷. In a W1 PCW, the optical mode profile spreads deeper into the photonic lattice with reduced group velocity^{5,8}. This lateral spread reduces optical confinement and increases propagation loss for slow light modes, which can weaken some of the benefits derived from the slow light effect. By contrast, in slotted PCW, optical confinement does not decrease with increased group index, as a result of the high index contrast in silicon platform. In a high index contrast interface, a transverse electric guided mode is required to have much higher intensity in the low index region. Consequently, when approaching the edge of the photonic band gap, the percentage of energy concentration in the low index slot will increase rather than decrease⁹. The increasing optical confinement with slower group velocity is a very advantageous property for compact optical communication devices⁹⁻¹⁹ and on-chip sensors^{20,21}. Despite these benefits, optical coupling between a strip waveguide and a slotted PCW is more challenging than conventional PCW due to the exotic mode profile and slow group velocity in the slotted PCW. Without a properly designed coupling interface, strongly confined guided mode profile with minimal overlap and large group index mismatch result in negligible coupling²². Efforts to improve the coupling efficiency include using a multi-mode interference (MMI) coupler²², changing the termination of the slot²³, and resonant coupling²⁴. However, MMI coupler only provides efficient coupling with limited bandwidth. Changing the slot termination position improves bandwidth²³, but with low overall transmission. Resonant coupler approach shows better coupling efficiency, but could not avoid a strong transmission dip \sim 10dB in the slow light region. By contrast, a theoretical study suggests that good coupling is achievable with good mode profile and group index matching¹⁶. Based on similar concept, we present a simpler design and experimentally demonstrate highly efficient coupling into slow light slotted PCW. We also study the effect of mode matching and group index matching experimentally, which offers more insights on the strip-slotted PCW coupling process.

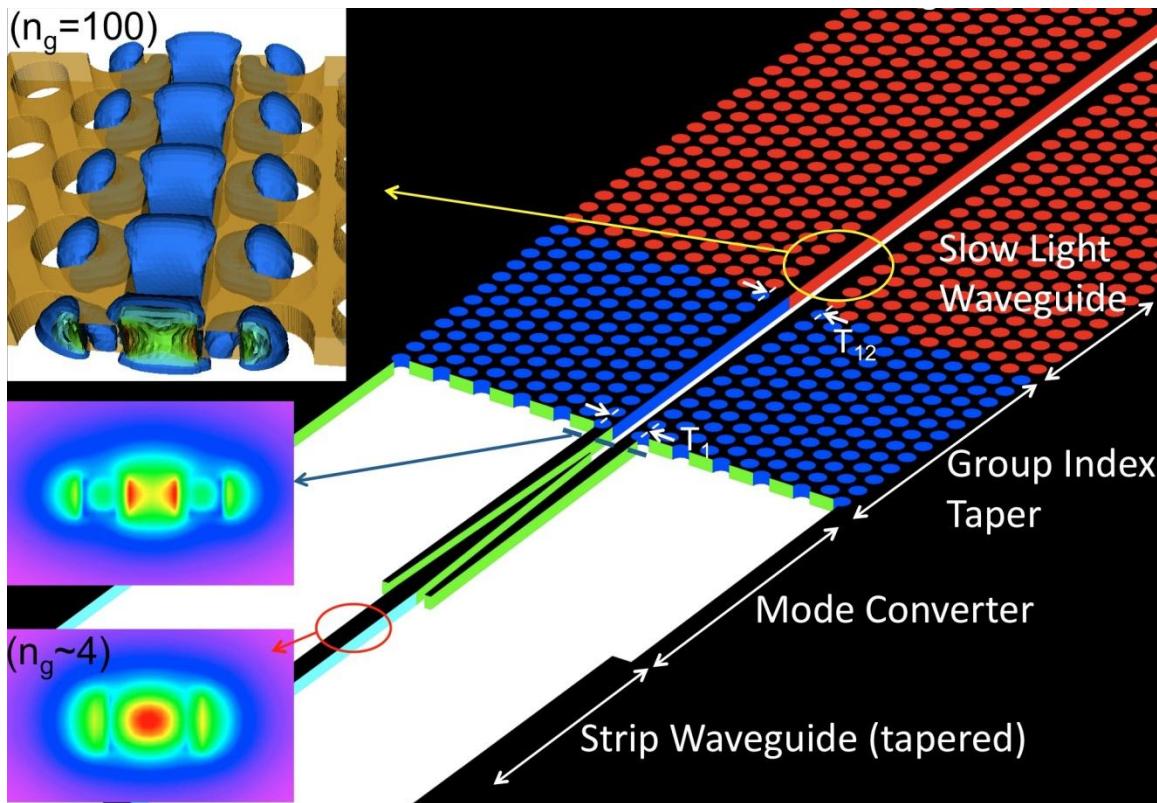


Figure 8 - 1. Schematic of the slow light slotted PCW, group index taper, mode converter, and strip waveguide (tapered). The insets show the mode profiles of a strip waveguide and a slow light slotted PCW at high group index ($n_g=100$).

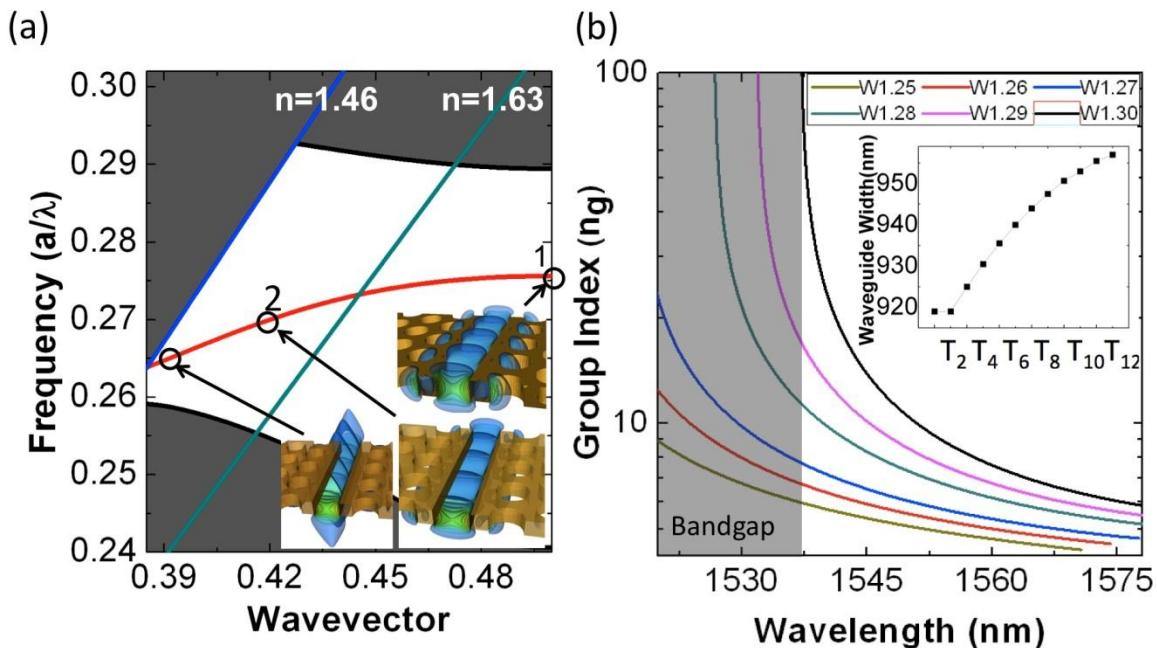


Figure 8 - 2. (a) Photonic band diagram. (b) Group index versus wavelength. The inset shows the waveguide width in the group index taper region.

8.1 Design of The Group Index Taper

The schematic of the slotted PCW is shown in Figure 8 - 1. The slotted PCW devices are formed by etching air holes and slots on a 230nm crystalline silicon nanomembrane sandwiched between a 3 μ m thick silicon dioxide layer ($n=1.46$) and a 2 μ m thick polymer layer ($n=1.63$), which serves as the bottom and top cladding layers, respectively. Air holes and slots are filled with the same material as the top cladding, which also prevents undesirable oxidation of the silicon layer. The lattice constant (a), air hole diameter (d), slot width (sw), silicon thickness (h) and line defect waveguide width (T_{12}) for the slow light waveguide are chosen to be $a=425\text{nm}$, $d=297\text{nm}$, $sw=320\text{nm}$, $h=230\text{nm}$, and $T_{12}=1.3\sqrt{3}a$ so that this waveguide supports a defect-guided mode that falls inside our experiment observation window of 1520~1610nm. The photonic band diagram for the slow light waveguide is shown in Figure 8 - 2 (a). The in-plane electric field distributions of the guided mode at wave vectors below and above polymer light line are also shown in the inset of Figure 8 - 2 (a). The radiation loss above polymer light line is small for the length of our devices. Therefore it is possible to have transmission between polymer light line ($n=1.63$) and oxide light line ($n=1.46$). This phenomenon was also verified experimentally as shown in Figure 7 - 4. To minimize the modal mismatch, we use an optical mode converter that can convert a strip waveguide mode into a conventional slot waveguide mode²⁵, which has a mode profile similar to that of a slotted PCW^{1,2,22}. To further improve mode profile matching with a strip waveguide, a wide slot width of 320nm is intentionally chosen, a maximum width that supports a mode size similar to that of a 340nm wide silicon strip waveguide. For a photonic crystal modulator operating in the slow light region, the increased slow light mode coupling efficiency and relaxed fabrication requirements compensate for the loss in optical confinement, leading to better overall performance with a wider slot^{9,10}. The group index mismatch can be adiabatically tuned by using a photonic crystal group index taper^{26,27} that provides a smooth transition in group index²⁶ as shown in Figure 8 - 2 (b). The taper is formed by parabolically reducing the width of a line defect waveguide from ($T_{12}=1.3\sqrt{3}a$) towards the coupling interface ($T_1=1.25\sqrt{3}a$) as shown schematically in Figure 8 - 1. The parabolic photonic crystal taper is designed by choosing a line defect waveguide width (T_1) that has lower group index than the slow light waveguide (T_{12}) over the entire guided mode spectrum followed by parabolic fitting to determine the waveguide widths ($T_2\sim T_{11}$) between them. The taper design uses unified hole size, which is much easier to realize than the taper in¹⁶. It is worth nothing that these design principles based on mode profile matching and parabolic group index taper should work for narrower slots as well. However, narrower slots are more sensitive to sidewall roughness due to higher field intensity

8.2 Fabrication of Four Test Structures

Slotted PCW devices were fabricated on a silicon-on-insulator wafer with 230nm top silicon layer and 3 μ m buried oxide. Details on the fabrication and characterization methods were described elsewhere^{9,10,27}. Four different designs were fabricated to experimentally study the effect of mode matching and group index matching in a strip waveguide-slotted PCW coupling. Scanning electron microscopy (SEM) pictures of the fabricated devices are shown in Figure 7 - 4.

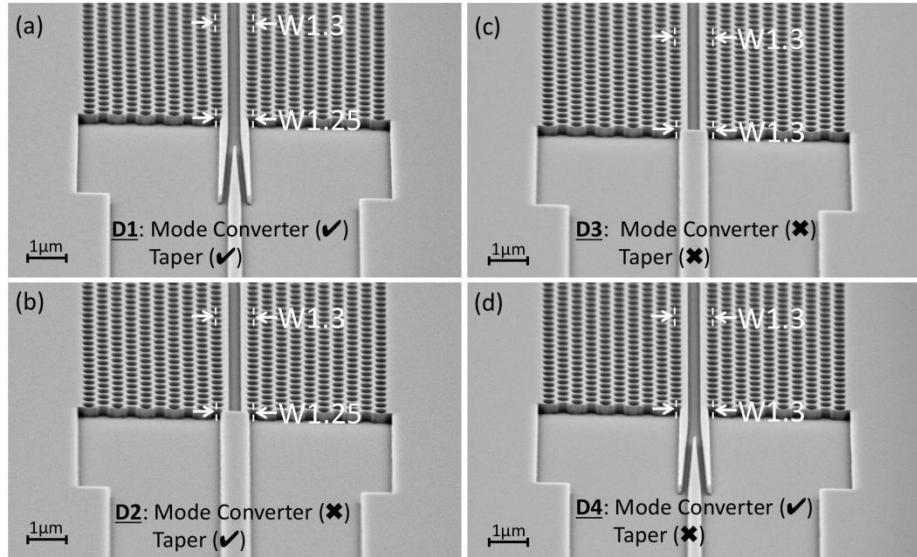


Figure 8 - 3. Scanning electron microscope (SEM) pictures of the fabricated slotted PCW devices.

8.3 Transmission Spectra Measurements

Figure 7 - 4 shows the comparison of transmission spectra measured from the four different devices (D1-D4) in Figure 8 - 3 and experimental n_g value calculated from the fringes in D4 using the method described in²⁸. These results highlight the importance of mode matching and impedance matching for achieving wide bandwidth, low loss, and group velocity independent coupling. Several distinct differences are observed in the transmission spectra. First, the transmission spectrum of D1 shows the best coupling efficiency, featuring minimum insertion loss of 2.4dB around 1546.5nm in reference to a strip waveguide of equal length on the same chip. Second, low frequency fringes due to Fabry-Perot reflections at the strip-Slotted PCW interface are suppressed. This results in a nearly flat and high transmission throughout the entire defect-guided mode spectrum. Third, comparing D1 to D4 demonstrates a 7 dB loss in coupling efficiency if group index matching is not achieved. Fourth, the comparison between D1 and D3 shows the loss in transmission can be as high as 13dB if both mode matching and group index matching are not attempted. Fifth, the transmission cut-off wavelengths of slotted PCW devices without mode converters (D2 and D3) happen at 1538.8nm and 1538.4nm, as opposed to 1537.3nm and 1537.4nm for devices that have mode converters (D1 and D4). It is known that cut-off wavelength is a unique property of the guiding region, which is identical for D1~D4. This result illustrates that the coupling loss for slow light can be very high for non-optimized structures. To make sure that this difference in cut off wavelengths is not a result of fabrication error, careful SEM inspection was performed on three sets of samples to confirm that all devices are identical in the slow light waveguide region. The same measurement was also repeated multiple times on each set of samples. All measurements show identical trends with minor variations. Finally, D2 shows the lowest coupling efficiency despite having the group index taper design. This is mainly due to the gradually decreasing waveguide width in the photonic crystal taper region. Without a mode converter to achieve mode matching, the narrower width of slotted PCW at the taper region can deteriorate the modal mismatch and cause low coupling efficiency when compared with the scenario shown in D3.

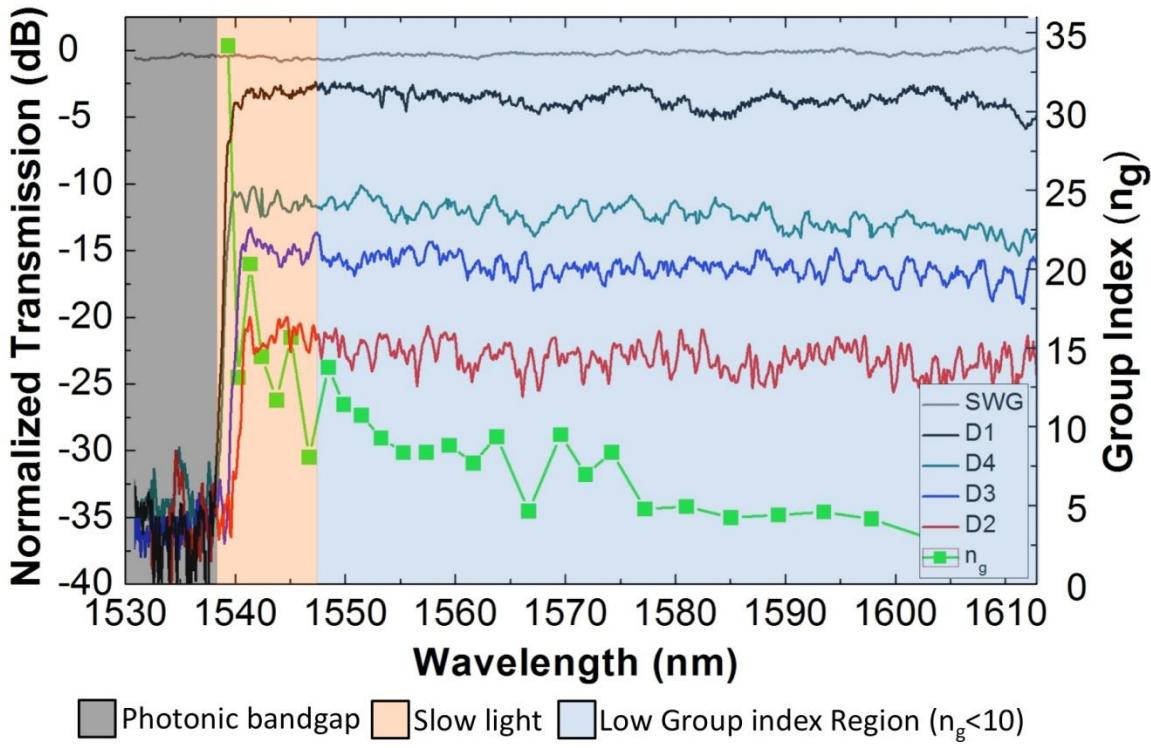


Figure 7 - 4. Transmission spectra of D1, D2, D3, and D4. SWG represents strip waveguide

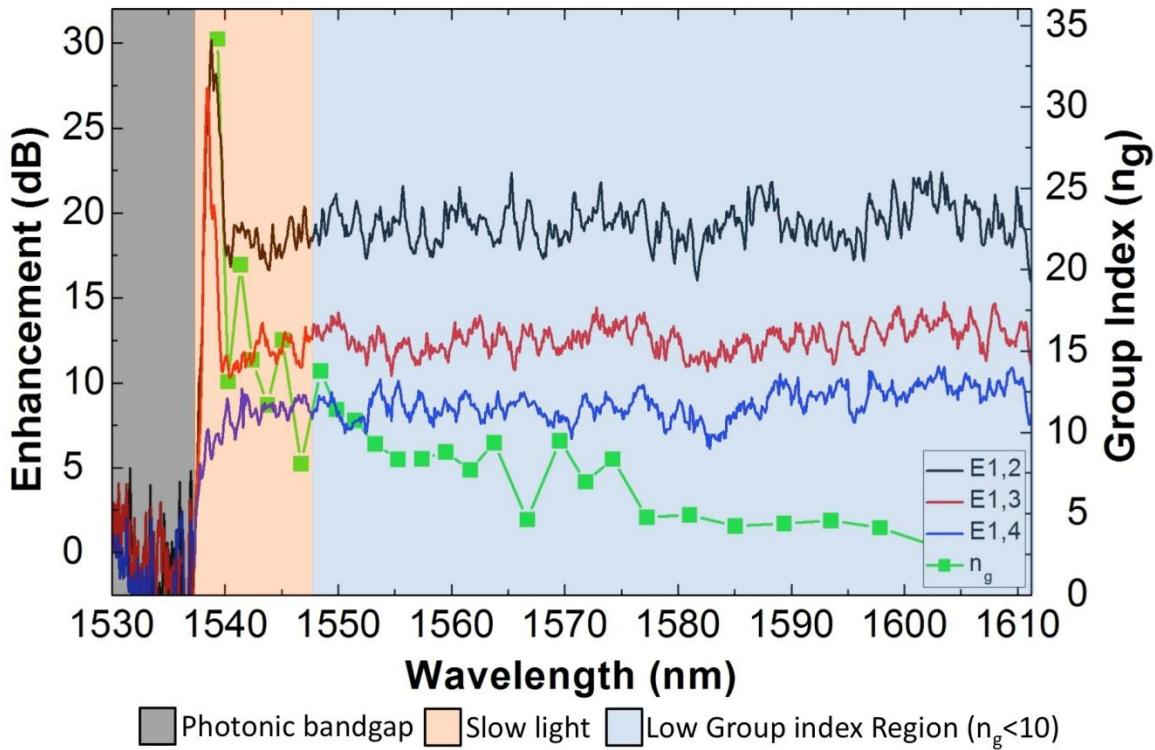


Figure 8 - 5. Enhancement spectrum defined as the transmission difference between device D1 and other devices.

In order to accurately depict the enhancement of coupling efficiency in the slow light region, we also show the difference in transmission between the best case of D1 and others (D2, D3, and

D4) together with group index. From Figure 8 - 5, one can see that the baseline in D1 is more than 17dB (E1,2 curve), 10dB (E1,3 curve), and 7dB (E1,4 curve) higher than D2, D3, and D4. The transmission enhancement in the high group index region around 1537nm~1541nm is even more significant. Curves E1,2 and E1,3 show strong enhancements of 30dB and 27dB within a 3nm and a 2nm spectrum next to the photonic bandgap. These results highlight the coupling efficiency enhancement in the most important region for the operation of slow light devices.

8.4 Conclusion

In conclusion, the experimental demonstration of efficient coupling into a slow light slotted photonic crystal waveguide is reported. Measurement results show up to 20dB enhancement in overall coupling efficiency and up to 30dB enhancement in the high group index region near the band edge. Suppression of low frequency fringes confirms that Fabry-Perot reflection at a strip-slotted PCW interface is minimized. A flat-top transmission spectrum and a 2.4dB insertion loss for a 34 μ m long slotted PCW represents the possibility to design devices that benefit from slow light enhancement without the classically high coupling loss associated with group index or modal mismatch.

8.5 Acknowledgement

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9.0 Silicon Nanomembrane Based Photonic Crystal Waveguide Array for Wavelength-Tunable True-Time-Delay Lines

Photonic crystal waveguides (PCWs) offer strong optical confinement, slow light enhanced interactions, and strong dispersions. These properties enable realization of many miniaturized and highly efficient devices such as hybrid silicon modulators¹⁻³, optical switches⁴, on-chip environmental sensors for underground water pollution detection⁵, and gas sensors for green house gas detection⁶. Recent studies have shown that PCWs can also be used to build optical delay lines^{7,8}. However, much of the reports in PCW delay lines have been focused on a single delay line rather than building a chip integrated module. The high dispersion and slow-light PCWs will greatly benefit the development of lightweight and compact systems. Specifically, for applications requiring strict control on payload, such as phased array antenna (PAA) systems⁹ in air-borne platforms, such miniaturized systems can enhance functionality while maintaining a minimum form factor. It is well known that photonic true-time-delay (TTD) systems enable broadband operation of PAA due to their inherent characteristic of providing a linear response of phase-frequency relationship across the entire operating bandwidth of the radio-frequency (RF) signal¹⁰. Furthermore, utilization of PCW TTDs can offer significant reduction in device footprint when operating in the high group index region. A TTD module based on PCW devices shall provide large bandwidth, small footprint, and large tunable time delay.

In this paper, we explore the utilization of a slow-light PCW for application in an X-Band TTD module. A broadband PAA with large steering angle and high directivity requires hundreds or even thousands of radiating elements. A TTD module with large and tunable time delay is required to control the phase of each radiating elements. To create large time delay, PCWs with lengths in mm range are often required. However, the large insertion loss of PCWs can be a prohibitive factor for building such long-length TTD devices. While the propagation loss can be minimized with better etch processes and post-etching oxidation treatment¹¹, minimizing coupling loss requires a special design to achieve a better mode matching at the strip waveguide-PCW interface. Previous demonstrations have achieved 80ps time delay with a 4mm long PCW when operated at group index $n_g=12.58$. In the work reported herein, we use a photonic crystal waveguide taper¹² to minimize coupling loss, which allows the delay lines to operate at a much higher group index that delivers much higher delay time with shorter physical length. Using the four-channel PCW array integrated with a 1x4 multimode interference (MMI) coupler, we experimentally demonstrate the first PCW-based chip-scale integrated TTD module with three continuously tunable true-time-delays covering the ranges of (6.72,65), (10.56,126.3), and (22.54,216.7) ps. The highest group index that we can perform phase-frequency measurement is ~23, which is calculated from the maximum time delay (216.7ps) measured in 3mm PCW.

The micrograph of the PCW TTD module is shown in Fig.9-1 (a). The optical input power is uniformly divided into four channels using a 1x4 multimode interference (MMI) beam splitter, which has a width and length of $16\mu m$ and $117.7\mu m$, respectively. The input and output access waveguides widths are $2.5\mu m$ on a 230 nm silicon nanomembrane on a silicon-on-insulator (SOI) wafer, which has been optimized for high MMI performance¹³. Each channel consists of carefully chosen lengths of silicon strip waveguides and PCWs¹², such that at any given wavelength within the bandwidth of interest, a constant time delay difference is setup between adjacent channels. Channel-1 contains a 5mm-long silicon strip waveguide and no PCW, and is chosen as a reference line. Channels-2, 3, and 4 contain 4mm, 3mm, and 2mm silicon strip waveguides and 1mm, 2mm, and 3mm-long PCWs, respectively, with identical PCW parameters. When the operating wavelength λ is tuned, this configuration creates proportional relative

time delay 0, t , $2t$, and $3t$ in channels 1~4, respectively. Note that since a different τ_i time delay difference is achieved for different tuning wavelength λ_i , the time delay profiles can provide appropriate phase distribution at the output for operation in a PAA. Scanning electron micrographs of the 1x4 MMI and the waveguide splitting section for four channels are shown in Fig.9-1 (b) and (c), respectively. The enlarged view of the slow light PCWs and the PCW taper regions are shown in Fig.9-1 (d) and (e), respectively.

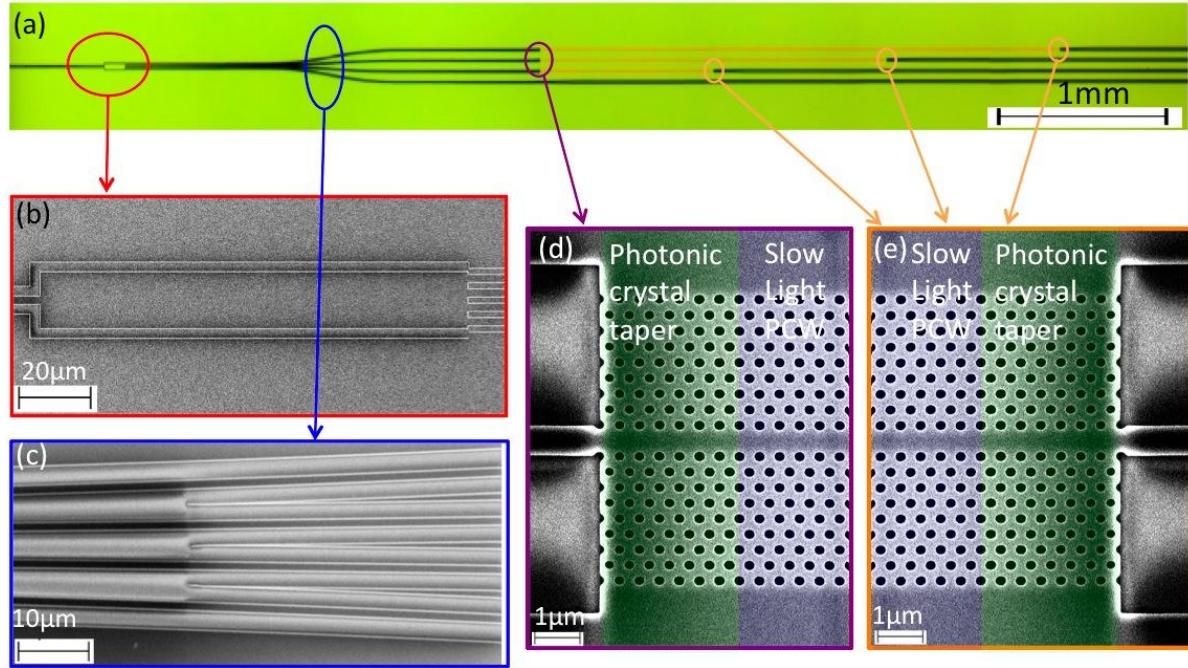


Fig.9-1(a) Microscope picture of the TTD beamformer based on a 1*4 MMI and PCWs. (b) SEM picture of the enlarged view of the 1*4 MMI power splitter. (c) Enlarged view of the S-bends that increase the waveguide separations. (d) and (e) SEM pictures of the PCW region containing photonic crystal taper and slow light PCW region.

In our design, the lattice constant (a), hole diameter (d), and slab thickness (h) of the W1 PCWs are chosen as 405nm, 190nm, and 230nm, respectively so that the PCWs support a guided mode covering 1533~1573nm. Detailed design parameters are covered in our previous work¹². To minimize the coupling loss into the slow light PCW, we utilize two photonic crystal tapers at the strip-PCW interfaces¹². These structures significantly improve the matching of the two different waveguide modes and reduce coupling loss. Such a design enables operation in the high-group index region near the band-edge, which gives much larger delay time and faster tuning based on wavelength tuning.

The on-chip TTD module is fabricated on a Unibond SOI wafer with a 250 nm top silicon layer and a 3μm buried oxide (BOX) layer. First, a 45 nm of thermal oxide is thermally grown as an etching mask for pattern transfer. Then, MMI power splitter, PCWs, photonic crystal tapers, and strip waveguides are patterned in one step with a JEOL JBX-6000FS electron-beam lithography system followed by reactive ion etching.

The TTD module is tested on a Newport 8-axis precision automated alignment station, which has a 10nm horizontal alignment accuracy and 5nm vertical alignment accuracy. In order to measure the output characteristics of the fabricated device, light from a broadband laser source is TE polarized and coupled to the TTD module through a polarization maintaining lensed fiber. The output signal from the TTD module is collected using single mode lensed fibers. Transmission spectra of the channels containing PCWs were also characterized to identify the transmission bands of the PCWs experimentally. Note that the measurement data were taken from integrated devices, i.e. the transmission through MMI and PCWs. Transmission spectra for channel-2~4 are shown in Fig.9-2, which clearly show overlapping transmission bands from 1533nm to 1573nm. Each set of data is composed of 1200 data points to ensure good accuracy, and the results for each of the channels from 2~4 were normalized to the transmission of the strip waveguide channel. The coupling loss of PCWs is significantly reduced due to the implementation of PCW tapers. The highest transmission point is -2.68dB for channel-2, which contains 1mm long PCW. The increasingly large fluctuation in the transmission spectra for longer PCWs channels are mainly due to the propagation loss from the fabrication related imperfections in the PCWs.

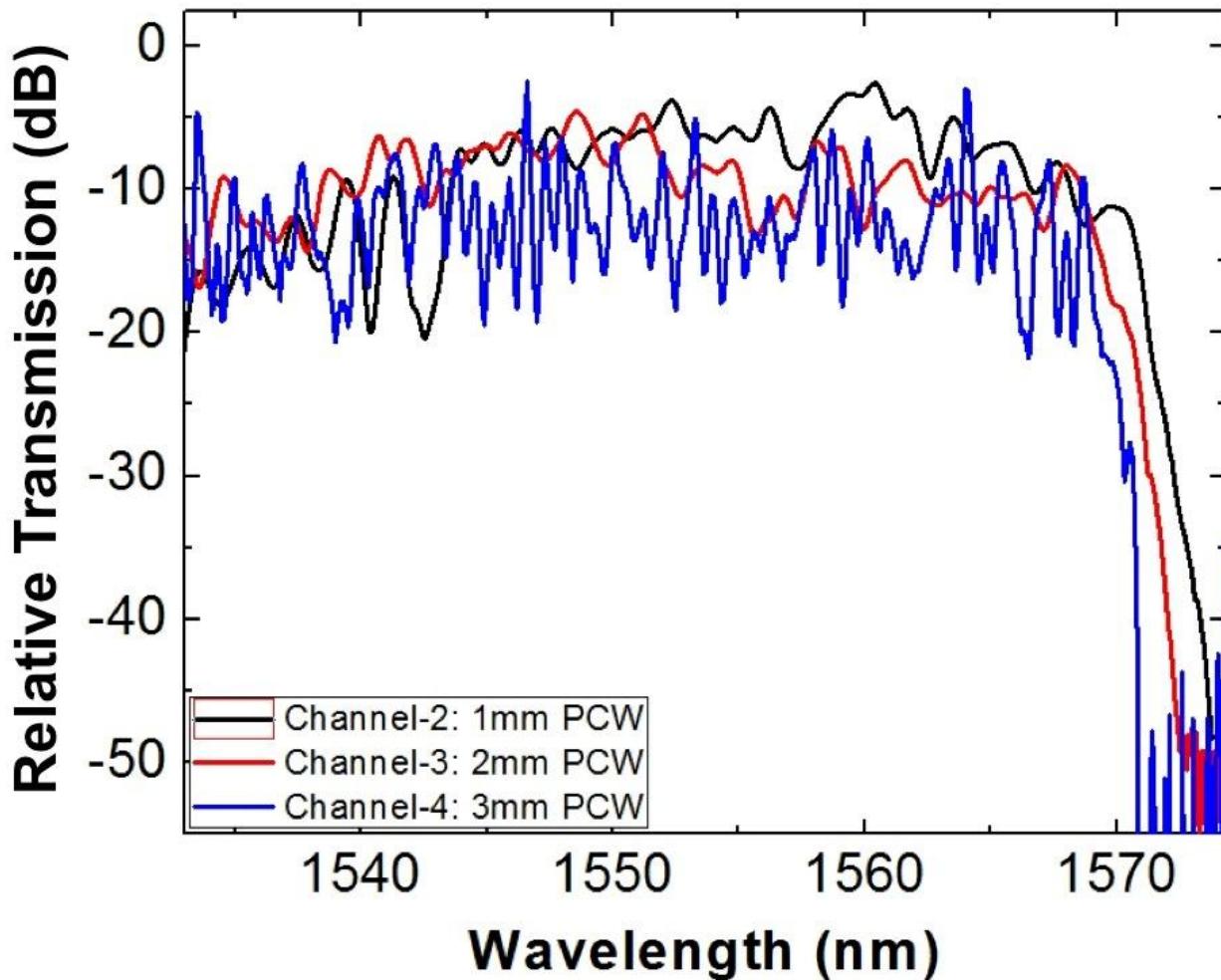


Fig.9-2 Transmission spectra of the channels containing 1~3mm PCWs.

The schematic of the measurement setup is shown in Fig.9-3 (a). In order to measure the time delay from the TTD lines, a X-band (8-12GHz) RF signal from an HP8510C vector network analyzer (VNA) is modulated onto an optical carrier from a tunable continuous wave laser by a LiNbO₃ modulator. The output of the modulator is coupled to the on-chip TTD module using the same method used to characterize the transmission spectra of TTD channels. A photodetector (PD) covering the X-band frequency range is used to convert the modulated optical signal to an electrical signal, which is then amplified using an X-band RF amplifier and fed back to the network analyzer. The time delay of the RF signal achieved in the TTD module for a given wavelength is obtained from the phase-frequency measurement using a VNA. The time delay from strip waveguide channel (channel-1) is subtracted from the measurement results in channel-2~4 to show the relative time delays in delay lines that contain PCWs. Due to the strong fluctuation in transmission spectra below 1545nm and above 1572nm, time delay measurements were only performed between 1545nm and 1572nm to avoid strong optical loss. The wavelength of the optical carrier is then tuned continuously from 1545nm to 1572nm. Because the group index increases with wavelength, the time delay also increases with wavelength accordingly. This phenomenon is shown in the increasing slopes in Fig.9-3 (b)~(d.) Highly linear phase-frequency relation is seen in all the channels, which clearly shows constant time delay for all frequencies-the signature of true-time-delay. This characteristic is critical to have a wide band phased array antenna without beam squint effect covering the whole X-band (8 to 12.5 GHz)¹⁴. The time delay (t) in the PCWs is derived from a linear regression fit following the relation $t = DF/DW$, where DF represents the changes of phase in the measurement frequency range DW . Accordingly, the maximum time delays obtained are 65ps, 126.3ps, and 216.7ps for channels-2, 3, and 4, respectively. The maximum relative time delay we measured (216.7ps) corresponds to a group index ~23, which represents the highest group index we can operate our delay lines under constraints such as propagation loss and pulse distortion related to strong dispersion in high group index mode.

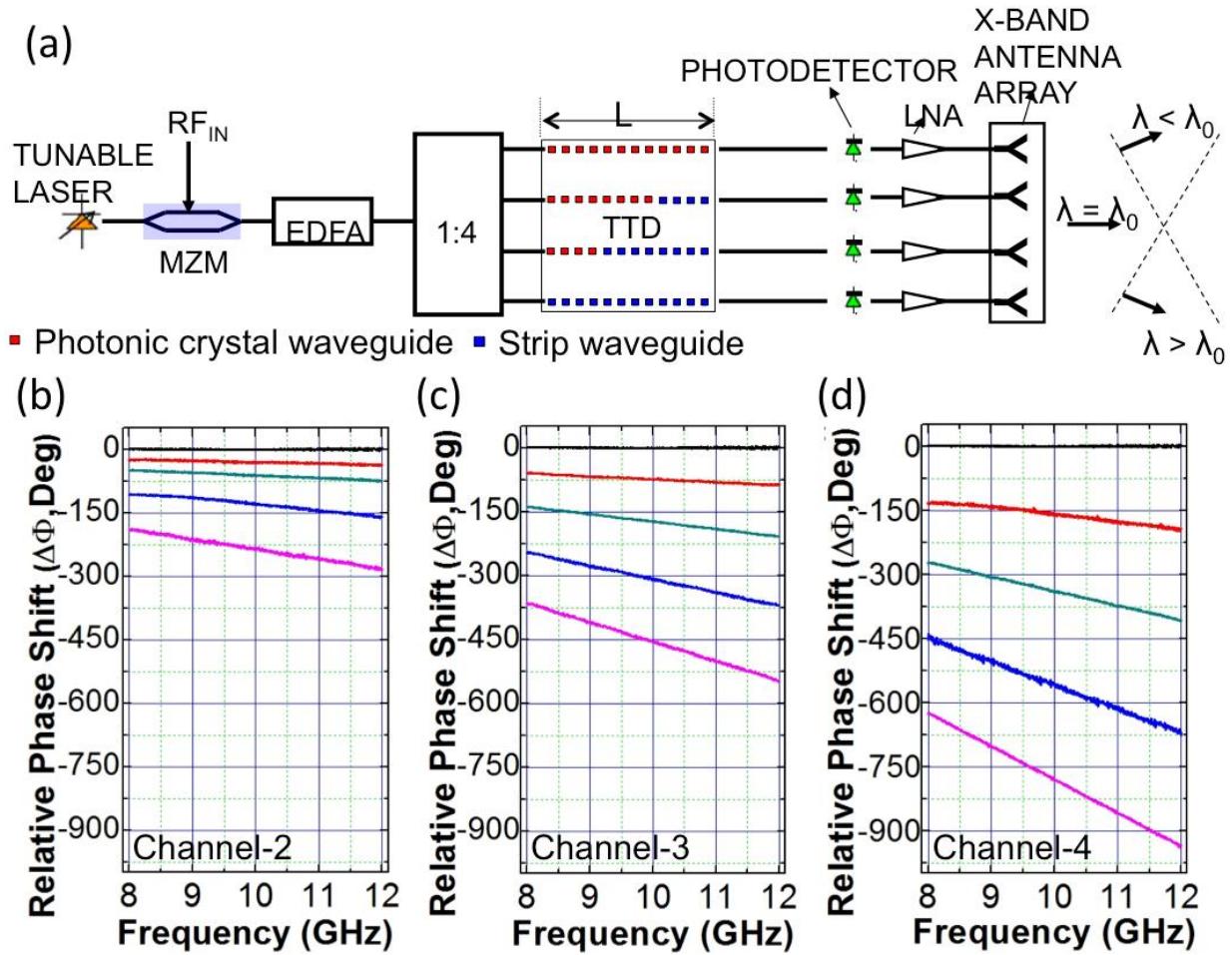


Fig.9-3 (a) A schematic of the measurement setup of a PCW-based TTD module. Measurement results of phase vs. frequency relation for (b) channel-2, (c) channel-3, and (d) channel-4. Measurement results were normalized to the strip waveguide (channel-1). The horizontal line (black) in (b), (c), and (d) represents the normalized phase shift of channel-1. From top to bottom, each color line represents the measurements performed at $\lambda=1548\text{nm}$, 1552nm , 1562nm , and 1568nm , respectively.

The wavelength-tunable time delay results are summarized in Fig.9-4. When external tunable delay lines are used to offset the time delay difference between adjacent delay lines, this TTD module can provide a steering angle from -44.38 degree to 44.38 degree if wavelength is tuned from a central wavelength $\lambda_0=1558.5\text{nm}$ for an X-Band PAA with inter-element spacing of 1.25cm. Further system demonstration containing a real X-band phased array antenna is under investigation and further results will be presented in the near future.

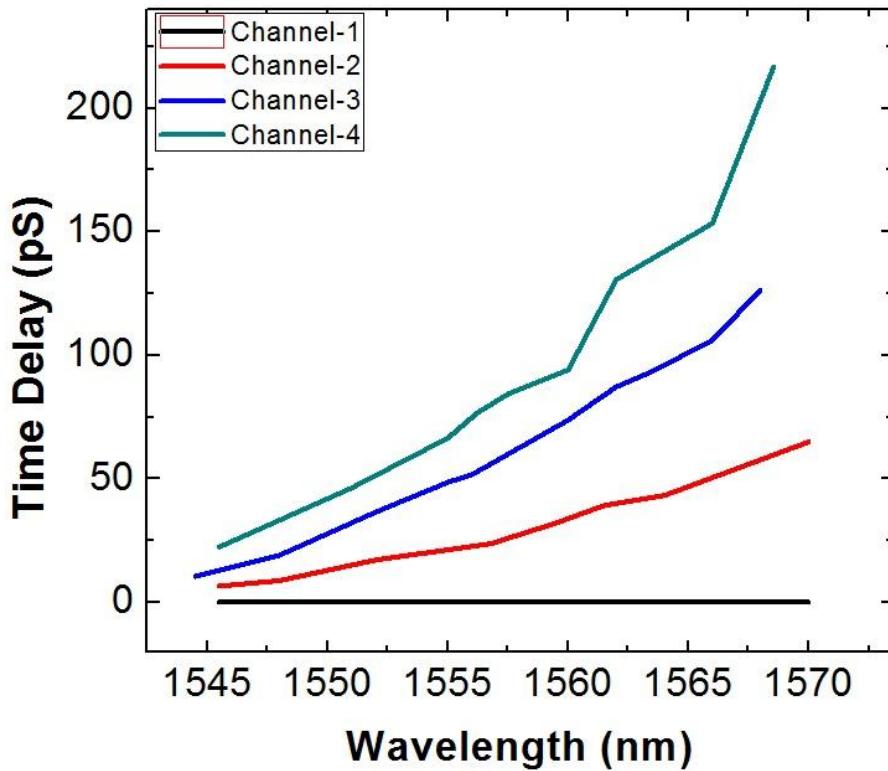


Fig.9-4 Wavelength-Tunable Time Delay for all four channels

In conclusion, we experimentally demonstrate a chip-scale four-channel TTD module based on slow light photonic crystal waveguides. The implementation of photonic crystal waveguide tapers enables device operation in the high group index region near the band edge, thus allowing access to much larger time delays. The integrated TTD module offers continuous wavelength tunable time delays up to 216.7ps for a PCW with a length of 3mm. Further optimization of the interfaces between MMI and PCWs can lead to lower optical loss, and better signal quality. The utilization of even longer PCW channels can cover time delays up to 1ns, which can accommodate more delay line channels and give better directivity. Such a compact device can be implemented in a broadband PAA system in order to achieve large steering angles within the whole X-band.

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10 Passive and active slow light photonic crystal structures

Wei Jiang

In this period, Jiang group at Rutgers University experimentally explored a slow-light odd mode in a photonic crystal waveguide. This odd mode is usually difficult to observe because its odd symmetry prohibits its excitation by the fundamental even mode of a typical waveguide. As such, very little is known regarding its loss and slow light characteristics. Here we study this odd mode to explore new possibilities of reducing slow light loss for delay line applications. This odd mode may also facilitate the development of novel mode-symmetry-transform devices, such as CMOS-compatible one-way waveguides. An odd-mode Mach-Zehnder coupler is introduced to transform mode symmetry and excite a high-purity odd mode with 20 dB signal contrast over the background. Assisted by a mixed-mode Mach-Zehnder coupler, slow-light mode beating can be observed, and is utilized to measure the group index of this odd mode.

In addition, we have studied thermo-optic characteristics of slow-light photonic crystal structures on a silicon-on-insulator wafer. The fundamental understanding of these characteristics is crucial for thermo-optic tunable delay lines. The power consumption and spatial temperature profile of such structures are given as explicit functions of various structural, thermal and optical parameters, offering physical insight not available in finite-element simulations. Agreement with finite-element simulations and experiments is demonstrated. Thermal enhancement of the air-bridge structure is analyzed. The practical limit of thermo-optic switching power in slow light PCWs is discussed, and the scaling with key parameters is analyzed. Optical switching with sub-milliwatt power is shown viable. The results given here can be adapted to optimize power consumption for thermo-optically tunable delay lines.

10.1. SLOW-LIGHT ODD MODE IN A PHOTONIC CRYSTAL WAVEGUIDE

10.1.1. Introduction

Photonic crystal waveguides (PCWs) can modify light propagation and dispersion characteristics through their periodic structures, thus have important applications in communications and sensing. Particularly, the slow light effect in a PCW can significantly enhance light-matter interaction, as demonstrated in significant reduction of interaction lengths for PCW based modulators and switches [1]. To date, most of the PCW research has been focused on the TE-like mode with even symmetry. However, a PCW often has an odd TE-like mode inside the photonic bandgap exhibiting the slow light effect as well. This odd mode can potentially open up the opportunities for mode-symmetry-based novel devices, such as one-way waveguides that exploit indirect interband photonic transitions between even and odd modes [2]. The slow light effect in PCWs can help reduce the interaction length for such transitions, enabling ultracompact devices. In addition, it may also open new routes to lower slow light loss. To utilize this odd mode in any devices, it is crucial to control its excitation symmetry and understand its slow light spectral characteristics. Normally, this odd mode does not exhibit itself evidently in the PCW transmission spectrum because its odd symmetry prohibits its excitation by the fundamental even mode of a conventional waveguide typically used at input. Symmetry-breaking structure imperfections sometimes may induce some coupling to this odd mode, causing a decrease of PCW transmission in the odd mode band [3,4]. Here we demonstrate a novel scheme to control the excitation symmetry for high purity transmission of this odd mode, and investigate the spectral signatures under various excitation symmetries.

10.1.2. Design and simulation

Consider a W1 PCW formed on a silicon-on-insulator (SOI) wafer by removing a row of air holes in a hexagonal lattice with lattice constant $a=400\text{nm}$, hole radius $r=0.325a$, and Si slab thickness $t=260\text{nm}$. The band diagram in Fig. 1(a) is calculated by 3D plane wave expansion. Below the lightline (for the oxide bottom cladding), the even TE-like mode has a flat dispersion relation with group index $n_g > 50$, and a narrow bandwidth ($<4\text{nm}$). In contrast, below the lightline, the odd TE-like mode has a much wider bandwidth $\sim 20\text{nm}$ with n_g down to ~ 15 . Such a moderate n_g range is favorable for many applications as various types of losses are reduced at lower n_g [5,6]. Furthermore, the dispersion relation of the TM-like guided mode usually crosses that of the even mode [5], as seen in Fig. 1(a). But the TM-like mode does not cross the odd mode in the region below the lightline in Fig. 1(a). For $\alpha a/2\pi c = 0.28 \sim 0.286$, only the odd mode is below the lightline.

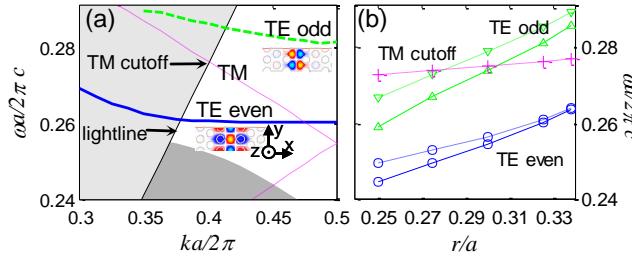


Fig. 1. (Color online) PCW photonic band structures. (a) Band diagram for $r=0.325a$. The dark grey region indicates the lower photonic band. H_z field profiles for even and odd modes at $k=\pi/a$ are shown in the insets (PCW axis along y). (b) Variation of the bandedge and cutoff of even (blue) and odd (green) TE-like modes with hole radius. For each TE-like mode, the lower line (solid) gives the bandedge; the upper line (dashed) gives the cutoff frequency where a mode crosses the lightline. The TM cutoff is also shown.

Systematic simulations show that as the hole radius increases, the odd-mode bandedge moves up faster than the TM cutoff, as shown in Fig. 1(b). For a sufficiently large r , the TM cutoff is below the odd mode bandedge; thus the two modes do not cross each other below the lightline, helping avoid their inter-coupling due to asymmetric top and bottom claddings. However, as r increases, the transmission bandwidth bounded by the bandedge and the cutoff decreases for both the even and odd modes, as shown in Fig. 1(b). Hence, this work focuses on the intermediate r case shown in Fig. 1(a), which shows a sufficient clearance between the odd mode bandedge and the TM cutoff, and a sufficiently wide bandwidth.

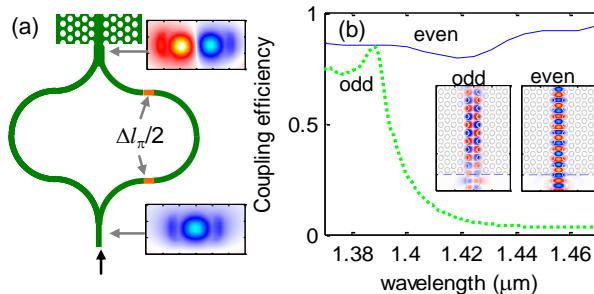


Fig. 2. (Color online) FDTD simulation results. (a) Schematic of the Mach-Zehnder coupler structure. The right arm has two extra waveguide segments (in orange) with a combined length of $(\Delta l)/\pi$. The input and output E_x field profiles (cross-section) are shown in the insets (200nm per division on axes). (b) PCW coupling efficiency. Insets: Coupled E_x field patterns at 1390nm. Light (in odd or even mode) enters from a Si waveguide at the bottom of each figure and into a PCW upward.

Excitation of this odd PCW mode is usually deterred by the opposite symmetry of the fundamental even mode of a Si waveguide. To solve this problem, we employ a two-step approach. First, a Mach-Zehnder coupler (MZC) whose two arms have a phase difference of π is utilized to transform mode symmetry and excite an odd mode in a wide (multimode) Si wire waveguide; then this odd mode is coupled to the odd mode of the PCW. To create π phase difference in this *odd-mode* Mach-Zehnder coupler, its two arms can be designed to have a length difference of $(\Delta l)_\pi = \lambda/2n_{\text{eff}}$, where n_{eff} is the effective index of the Si waveguide. Finite difference time-domain (FDTD) simulation has been performed to confirm that such a MZC produces an odd mode in a wide output waveguide, as shown in Fig. 2(a). The input and output waveguide widths are 400nm and 700nm respectively. The coupling between the odd mode of a Si wire waveguide (700nm wide) and that of the PCW is also simulated. Simulation results in Fig. 2(b) show coupling efficiencies up to $\sim 84\%$ ($\sim 0.75\text{dB}$) for the odd mode. The field pattern in Fig. 2(b) left inset confirms that the coupled PCW mode is an odd mode. The fundamental even mode of a Si wire waveguide couples into the PCW with inconsequential change of coupling efficiency for the spectral range in Fig. 2(b). The field pattern in Fig. 2(b) right inset indicates that the coupled mode has even symmetry. Indeed, this mode is an even TE-like mode above the lightline. The E_x field has been shown in Fig. 2 for direct comparison with the modes of the conventional Si waveguide, whose TE-modes are commonly visualized by E_x (note E_x and H_z have the same symmetry with respect to x).

10.1.3. Fabrication and characterization

The photonic crystal waveguide structure is fabricated on a SOI wafer with a $2\mu\text{m}$ buried oxide layer and a 260nm top Si layer according to the parameters used in Fig. 1(a). The structure is patterned by a JEOL JBX-6300FS high-resolution e-beam lithography system, operating at 100keV, on a 100nm thick layer of ZEP 520A e-beam resist. Then the pattern is transferred to the Si layer by an Oxford Plasmalab 100 ICP etcher. Fig. 3 is a scanning electron microscope (SEM) image of the fabricated structure. Two MZCs with a $10\mu\text{m}$ bending radius are connected through 700nm-wide Si waveguides of $1\mu\text{m}$ lengths to both ends of the PCW.

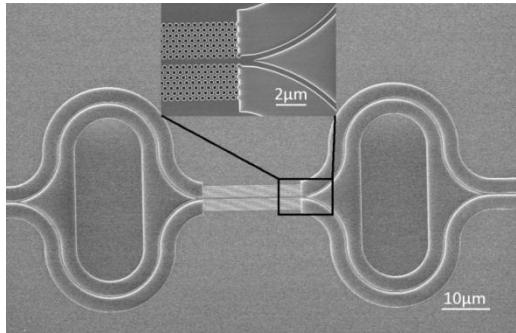


Fig. 3. SEM image of a PCW with odd-mode Mach-Zehnder couplers. Inset: close-up view of the coupling region at one end of the PCW.

To measure transmission spectra, light from a super-luminescent LED with a spectral range of about 80nm is coupled to the TE mode of Si access waveguides (tapered to $4\mu\text{m}$ at chip edges) via lensed fibers. A polarizer is used at the output end to block TM polarization. The PCW insertion loss is measured with reference to a Si wire waveguide. Fig. 4(a) shows the spectrum of a PCW with odd-mode MZCs. A substantial transmission bandwidth is observed, approximately 22nm at 10dB below the peak. The contrast between the transmitted mode and background is $>20\text{dB}$. The peak insertion loss is about -4dB . Separate measurements show that each Mach-Zehnder coupler contributes $\sim 1\text{dB}$. Thus the loss due to the PCW is estimated $\sim 2\text{dB}$. Considering the simulated 0.75dB coupling loss per PCW interface, the propagation loss is estimated around 0.5dB . For comparison, the spectrum of a directly coupled PCW

without MZCs is shown in Fig. 4(b). The transmission is due to the leaky even TE-like mode as simulated in Fig. 2(b). Figure 4(b) also shows the PCW transmission with Mach-Zehnder couplers whose two arms have a length difference Δl deliberately designed to be 50% greater than $(\Delta l)_\pi$. Such a *mixed-mode* Mach-Zehnder coupler offers a symmetry configuration that can excite a mixture of even and odd modes according to $I_\pm \propto (1/2)[1 \pm \cos(2\pi n_{\text{eff}} \Delta l / \lambda)]$. As such, the background transmission due to the even mode rises. In the odd mode band, the mixed-mode spectrum oscillates strongly due to the beating of two modes. Figs. 4(a)-(b) illustrate that distinctive spectral signatures can be observed with controlled excitation symmetries.

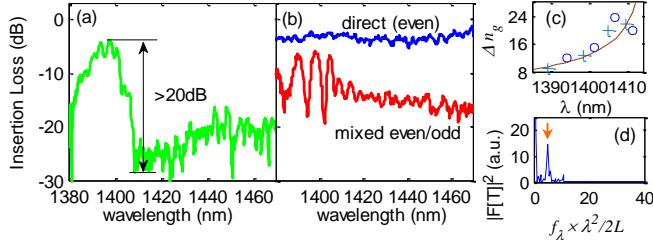


Fig. 4. (Color online) Transmission spectra for $20\mu\text{m}$ long PCWs: (a) with odd-mode MZCs; (b) direct transmission without MZC, and transmission with mixed-mode MZCs. (c) Δn_g obtained from the mixed-mode spectrum; the solid line delineates the trend. (d) Fourier transform of the transmission spectrum of another directly coupled PCW (the peak position gives $n_{g,\text{even}}$).

The mode-beating pattern of the mixed-mode spectrum contains important information of the odd mode. The beating period is related to the group indices of even and odd modes through $\Delta\lambda = \lambda^2 / (n_{g,\text{odd}} - n_{g,\text{even}})L$, where L is the PCW length. Simulation indicates that $n_{g,\text{even}}$ is virtually a constant (~ 5) in the odd mode band. Thus the chirped beating periods are due to the dispersion of $n_{g,\text{odd}}$. We have calculated $\Delta n_g = n_{g,\text{odd}} - n_{g,\text{even}}$ from the mixed-mode spectrum and plotted it in Fig. 4(c). The peak-spacing and valley-spacing of the spectrum give two sets of Δn_g data, plotted by circles and crosses respectively. They agree with each other as expected. Note that the Δn_g value obtained from two adjacent peaks (valleys) is assigned to the mid-point wavelength in-between. Further, $n_{g,\text{even}}=4.9$ is obtained in Fig. 4(d) through the Fourier transform of the transmission spectrum of another directly coupled PCW with more obvious spectral ripples. Note that the Fourier frequency f_λ is just the inverse of the spectral oscillation period $\delta\lambda$, thus $n_{g,\text{even}}=f_\lambda \times \lambda^2/2L$. Based on Fig. 4(c)-(d), we find $n_{g,\text{odd}}=\Delta n_g+n_{g,\text{even}}$ in the range of 14~29. Note that the F-P oscillation amplitude in Fig. 4(a) is relatively weak. In contrast, the mode-beating amplitude of the mixed-mode spectrum in Fig. 4(b) is much higher and more robust against noise, which facilitates the evaluation of $n_{g,\text{odd}}$. Also note that in Fig. 4(a), the background transmission increases discernibly beyond 1430nm due to the dispersive effect in the odd-mode MZC, which modifies the phase shift difference between the two arms as λ deviates far from the designed value (1390nm). The TM-like mode (guided for $\lambda > 1.45\mu\text{m}$) may also contribute to the background at long wavelengths. However, these effects are much weaker for 1380~1415nm.

10.1.4. Discussion and summary

Although this work focuses on PCWs on a SOI chip, the Mach-Zehnder coupler and the mode-beating based $n_{g,\text{odd}}$ measurement method can be adapted to the cases of air-bridge or oxide-covered PCWs, and coupled-cavity PCWs. The odd mode wavelength can also be shifted to $\sim 1550\text{nm}$ or other values (depending on specific applications) by changing the lattice constant. Furthermore, the understanding of the slow light and mode-beating characteristics of this odd mode, and the controlled excitation and $n_{g,\text{odd}}$ characterization schemes developed here can

facilitate the development of mode-symmetry based novel devices, such as one-way waveguides that involve active transition and passive conversion between even and odd modes [2]. Slow light can help reduce device interaction length. Lastly, the investigation of this odd mode may lead to new routes towards lower slow light loss.

In summary, we have experimentally demonstrated the control of excitation symmetry for an odd TE-like mode in a PCW. An odd-mode Mach-Zehnder coupler is utilized to selectively excite the odd mode with a contrast $>20\text{dB}$ over the background. Assisted by a mixed-mode MZC, slow-light mode beating is observed and is utilized to measure the group index of this odd mode.

10.2. THERMO-OPTIC CHARACTERISTICS OF SLOW-LIGHT PHOTONIC CRYSTAL WAVEGUIDES

Thermo-optic tuning is a useful technique for optical switches and tunable delay line applications. A photonic crystal thermo-optic device on an SOI chip comprises structural components whose scales differ by orders of magnitude, such as small holes of $\sim 200\text{nm}$ in diameter and thick substrates of hundreds of microns. Simulations of such a multi-scale structure can be time-consuming and challenging. Such simulations may be performed for a small number of structures. However they are not efficient for systematically studying a large ensemble of structures in which many parameters such as the hole diameter and the buried-oxide thickness vary over a large range. Here we develop an efficient and accurate approach to analyze the thermo-optic characteristics of an SOI photonic crystal structure. The effective thermal conductivity κ_{eff} for a silicon photonic crystal slab is determined through the lateral thermal spreading length. Physical properties such as the spatial temperature profile and the power consumption required to induce a π phase shift can be described semi-analytically based on a quasi-1D model with numerically determined κ_{eff} . The results agree well with 3D simulations based on the finite element method (FEM). The theoretical results also explain the low switching power observed in an air-bridge structure [7]. The analytic formulas offer insight into the key factors governing the thermo-optic characteristics of SOI photonic crystal structures.

10.2.1. Analysis of SOI photonic crystal thermo-optic structures

Fig. 5 illustrates two common configurations of active photonic crystal waveguide (PCW) structures on an SOI wafer. A heat source of width W and length L is assumed to be embedded in the top silicon layer. Such a heat source can be formed by a lightly doped (e.g. $\sim 10^{14}\text{cm}^{-3}$) Si strip surrounded by a relatively highly doped (e.g. $\sim 10^{17}\text{cm}^{-3}$) silicon on both sides [7]. Passing current laterally through this structure produces concentrated ohmic heating in the center strip.

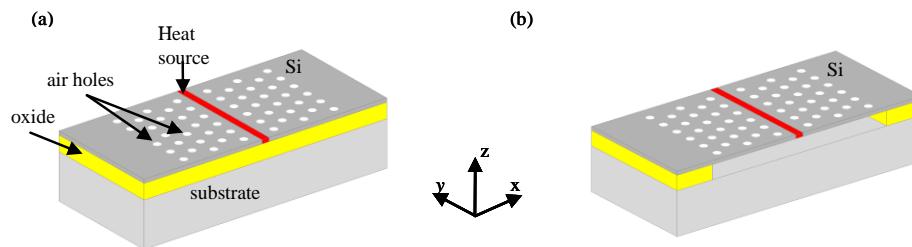


Fig.5. Configurations of Si active PCW structures. (a) SOI; (b) Air-bridge (membrane).

The heat conduction process in a photonic crystal slab can be effectively modeled by that of an equivalent hole-free homogeneous slab with an effective thermal conductivity κ_{eff} . This is

valid because the temperature varies spatially on a scale much larger than the typical photonic crystal lattice constant a . To determine κ_{eff} , the heat transfer process is simulated using the finite element method for one period of the PCW structure, as shown in the inset of Fig. 6. The thicknesses of the top Si layer and buried oxide layer are $t_{Si}=250$ nm and $t_{ox}=2 \mu\text{m}$ respectively. The hexagonal lattice has a lattice constant $a=400\text{nm}$. The simulations indicate that the vertical temperature variation in the top Si layer and the in-plane temperature variation in each unit cell are small. The temperature of the top Si layer varies significantly only along the x axis, as plotted in Fig. 6. Outside the heater (centered at $x=0$), it closely follows an exponential form

$$T(x) \approx \exp[-(|x|-W/2)/X_{spr}(r)] \quad \text{for } |x| > W/2, \quad (1)$$

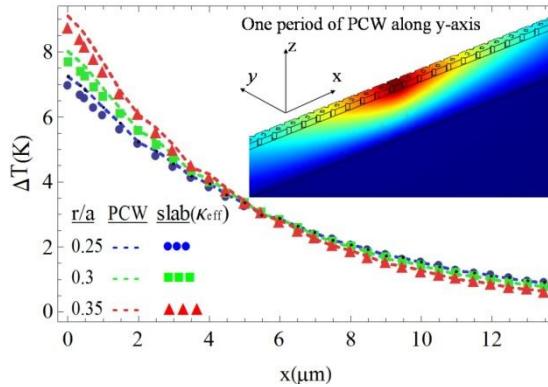


Fig. 6. Temperature profiles in the top Si layer of a PCW (center: $x=0$) for various hole radii and in a homogenized slab with $\kappa_{\text{eff}}(r)$. Inset: 3D temperature profile in a PCW with $r/a=0.25$. One period of the PCW along the y axis is shown.

where $X_{spr}(r)$ is the thermal spreading length. For an unpatterned SOI structure, it is given by [8]

$$X_{spr} = X_{Si} = [t_{Si}t_{ox}\kappa_{Si}/\kappa_{ox}]^{1/2}, \quad (2)$$

where κ_{Si} and κ_{ox} are the thermal conductivities of silicon and SiO_2 respectively.

For a photonic crystal slab, $X_{spr}(r)$ depends on the hole radius r and it can be obtained from an exponential fit of the lateral temperature profile in the slab. The effective thermal conductivity of a Si photonic crystal slab can then be calculated from

$$\kappa_{\text{eff}}(r) = \kappa_{ox}X_{spr}^2(r)/(t_{Si}t_{ox}). \quad (3)$$

The values of $\kappa_{\text{eff}}/\kappa_{Si}$ and X_{spr} determined from the plots are given in Table 1. To further verify the results, homogenized slab structures with the tabulated $\kappa_{\text{eff}}(r)$ are simulated, with all other parameters unchanged. The lateral temperature profile in the homogenized slab is generally in good agreement (within 6%) with that of the original photonic crystal slab, as shown in Fig. 6.

Table 1. Values of $X_{spr}(r)$ and $\kappa_{\text{eff}}(r)$ for various hole sizes.

r/a	0.25	0.275	0.3	0.325	0.35
$X_{spr}(\mu\text{m})$	6.3	6.0	5.7	5.3	4.9
$\kappa_{\text{eff}} / \kappa_{Si}$	0.68	0.61	0.55	0.48	0.41

For an SOI structure, the heat conduction can generally be described by a quasi-1D model predicated on the vertical heat conduction in the buried oxide [8]. Note that the thermal

spreading increases the effective heat flux cross-section to $A_{eff}=L[W+2X_{spr}]$. For the photonic crystal structure in Fig. 5(a), this model yields

$$Q = \kappa_{ox} L [W + 2X_{spr}(r)] (\Delta T_{ox} / t_{ox}), \quad (4)$$

where Q is the heat transfer rate (equal to the heating power in steady state) and ΔT_{ox} the temperature difference between the top and bottom of the oxide at $x=0$. To verify Eq. (4), 3D FEM steady-state simulations are performed for an SOI chip having a homogenized top layer with κ_{eff} (Fig. 7 inset). The absence of small holes significantly mitigates the difficulty in mesh generation for multi-scale structures, and reduces the simulation time significantly.

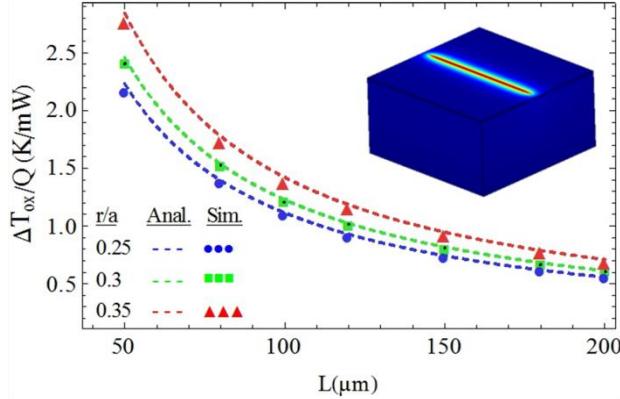


Fig. 7. $\Delta T_{ox}/Q$ vs. waveguide length L (for $t_{ox}=2\mu\text{m}$). Inset: 3D temperature distribution in a chip obtained from finite element simulation for a PCW structure having $t_{Si}=250\text{nm}$, $W=400\text{nm}$, $t_{ox}=2\mu\text{m}$, $\kappa_{eff}(r=0.25a)$ on a $200\mu\text{m}\times200\mu\text{m}$ substrate with a thickness of $100\mu\text{m}$.

Due to the small thermal conductivity and natural convection coefficient of air [9], the heat dissipation from the top and side surfaces of the chip is negligible, hence adiabatic boundary conditions are used for the top and side surfaces. The bottom surface is kept at 300 K. The simulated ΔT_{ox} per unit heating power Q and the results based on Eq. (4) agree well (within 3%), as shown in Fig. 7 for various lengths of the heat source.

10.2.2. Thermo-optic characteristics and switching power for SOI and air-bridge structures

To study the thermo-optic characteristics, we note that the phase shift induced in a PCW is given by [1]

$$\Delta\phi = 2\pi\Delta n \sigma L n_g / (n\lambda), \quad (5)$$

where n_g is the group index of the mode, λ the wavelength, and σ the fraction of the mode energy stored in the region where the refractive index change $\Delta n=(dn/dT)\Delta T$ occurs. By virtue of Eqs. (4) and (5), the power required to induce a phase shift of π for a structure in Fig. 5(a) is given by

$$Q_\pi = n\lambda\kappa_{ox}[W + 2X_{spr}(r)]/[2\sigma\kappa_{ox}n_g(dn/dT)]. \quad (6)$$

Because $X_{spr} \sim \sqrt{t_{ox}}$, the power Q_π actually scales as $1/\sqrt{t_{ox}}$ for heater width $W \ll X_{spr}$. Figure 8 shows the results for $\sigma = 0.9$, $\lambda = 1.55\mu\text{m}$ and $dn/dT = 1.86 \times 10^{-4} \text{ K}^{-1}$ with different values of oxide layer thickness. For $n_g=60$, $r/a=0.25$ and $t_{ox}=2\mu\text{m}$, Q_π is less than 2.5mW.

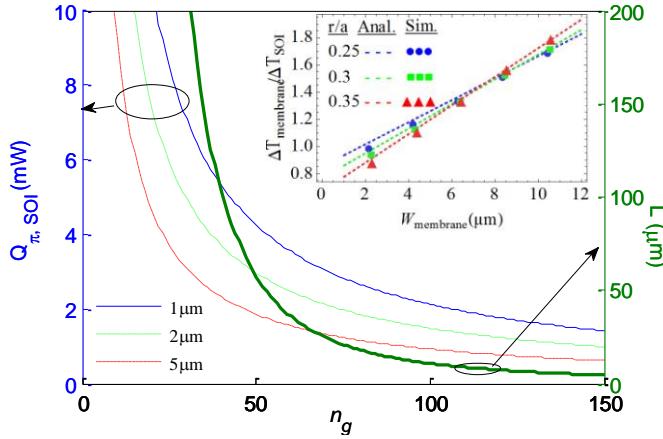


Fig. 8. Q_π vs. group index (n_g) for $r/a=0.25$ for an SOI PCW structure (for various t_{ox}), and the estimated 3dB-propagation-loss length for a membrane PCW structure. Inset: The thermal enhancement for a membrane PCW with $t_{ox}=2\mu\text{m}$.

This approach can also be applied to an air-bridge (membrane) structure shown in Fig. 5(b). Here the heat conduction consists of two steps in series: (1) the lateral heat conduction in the suspended membrane; and (2) the quasi-1D heat conduction in the SOI region. Based on the continuity of heat flux, one readily finds for the left (or right) half membrane

$$Q_{\text{membrane}}/2 = \kappa_{\text{eff}} L X_{Si} \frac{(\Delta T)_{\text{membrane}} - (\Delta T)_{\text{edge}}}{W_{\text{membrane}}/2} = \kappa_{ox} L X_{Si} \frac{(\Delta T)_{\text{edge}}}{t_{ox}}, \quad (7)$$

where W_{membrane} is the membrane width, X_{Si} is given by Eq. (2), $(\Delta T)_{\text{membrane}}$ is the membrane temperature rise evaluated at the PCW core and $(\Delta T)_{\text{edge}}$ at the membrane edge. Eliminating $(\Delta T)_{\text{edge}}$, we find

$$Q_{\text{membrane}} = \kappa_{ox} L (2X_{Si}) \frac{(\Delta T)_{\text{membrane}}}{t_{ox}} \frac{\kappa_{\text{eff}}(r) X_{Si}}{\kappa_{\text{eff}}(r) X_{Si} + \kappa_{Si} W_{\text{membrane}}/2}, \quad (8)$$

For the same power Q , the membrane structure may enhance the temperature rise by a factor

$$\frac{(\Delta T)_{\text{membrane}}}{(\Delta T)_{SOI}} \approx \frac{X_{spr}(r)}{X_{Si}} \frac{\kappa_{\text{eff}}(r) X_{Si} + \kappa_{Si} W_{\text{membrane}}/2}{\kappa_{\text{eff}}(r) X_{Si}}. \quad (9)$$

Correspondingly, Q_π of the membrane structure is reduced by this factor. The enhancement factors obtained from Eq. (9) agree very well (within 6%) with the simulation results, as shown in Fig. 8 inset. Based on Fig. 8, the attainable power consumption for a Si air-bridge PCW thermo-optic Mach-Zehnder switch is estimated between 1~2mW for $n_g\sim 60$ and $t_{ox}=2\mu\text{m}$, which agrees well with the experimental result [7].

10.2.3. Discussion

The scaling of the thermo-optic characteristics of an SOI photonic crystal structure with various parameters is of significant interest in device design. The analytic formulas enable us to study such scaling over a wide parameter range. The heater location is an important factor in determining the power consumption. Here we consider two options: in the PCW core [7], at the lateral edge of the PCW [10]. The temperature profile given in Eq. (1) shows that the temperature rise in the silicon layer decreases exponentially with the lateral distance from the

heater. Compared to a heater embedded exactly in the PCW core, a heat source located at $\Delta x=6\mu\text{m}$ from the core has an efficiency reduction by $\exp(-6\mu\text{m}/X_{spr})\approx 0.3\sim 0.4$ for $r/a=0.25\sim 0.35$. The buried oxide thickness is another crucial factor. Generally, a thicker oxide is preferred for lower power consumption according to Eqs. (6) and (8). However, the thermal time constant of an SOI chip increases with the oxide thickness. Therefore, some trade-off must be made in realistic device design to balance power consumption and speed. For the membrane structure, the enhancement factor in Eq. (9) is found to weaken the scaling of Q_π with t_{ox} due to $X_{Si} \sim \sqrt{t_{ox}}$. Thus, Q_π scales slower than $t_{ox}^{-1/2}$, particularly for a large $W_{membrane}$. Ultimately, the reduction of Q_π based on the slow light effect is limited by optical loss, which increases with n_g . The optical loss of a PCW can be attributed to a number of factors, such as random variation of hole positions due to fabrication tolerances, sidewall roughness, and the input/output coupling. The random variation of the hole positions in fabricated PCWs can be controlled to be within a small range ($<1\text{nm}$) with high-end e-beam lithography tools [11]; and the corresponding loss is usually small. Sidewall roughness of the holes depends on the lithography tool, resist, and etching process and is more difficult to control. Such roughness could induce substantial loss at large n_g . The estimated PCW length for 3dB propagation loss is plotted against n_g in Fig. 8 based on theoretical calculations with experimentally achievable rms roughness $\sigma=3\text{nm}$ and correlation length $l_c=40\text{nm}$ [6]. To further address the effect of the input/output coupling loss, we consider two prior experiments. In an earlier experiment [7], the insertion loss of well-fabricated PCWs is about 10~13dB at $n_g\sim 110$ for $L=50\mu\text{m}$ and $250\mu\text{m}$ and shows weak dependence on the PCW lengths. This indicates that most of the observed loss is due to input/output coupling [7]. A more recent experiment based on group index tapering has shown that the coupling loss can be significantly reduced throughout the spectrum of the defect-mode, including the slow light region near the band edge [12]. To summarize, with the best fabrication tools and best design, optical loss due to random hole position variation and input/output coupling can be very small, but the roughness induced loss [6] (especially the backscattering loss, which scales roughly as n_g^2) will be a primary limiting factor. Hence the roughness-induced loss (including backscattering and out-of-plane scattering loss) is considered in Fig. 8 to explore the limit of Q_π in connection with n_g . Considering all the factors discussed above, a practical lower limit of Q_π is estimated on the order of 0.5mW for a reasonable $t_{ox}\sim 5\mu\text{m}$, $L\sim 10\mu\text{m}$, and $n_g\sim 110$. Our calculation also shows that for $n_g\sim 60$, Q_π already enters the sub-milliwatt regime for the $t_{ox}\sim 5\mu\text{m}$ case.

It should be noted that this theory indicates that many factors are insignificant. For example, Q_π is insensitive to the choice of the heater width W as long as $W \ll 2X_{spr}(\sim 12\mu\text{m})$. Also, Q_π varies only ~20% for the typical radius range of $r/a=0.25\sim 0.35$. Note that typical silicon photonic crystal waveguides used for the 1550nm communications window have $a=380\text{nm}$ to 440nm . As the lattice constant is much smaller than the scale of temperature variation ($a \ll X_{spr}$), this approach works well for this range of a . For a given lattice structure, when a and r vary simultaneously while maintaining a fixed ratio of r/a , X_{spr} is essentially invariant.

10.2.4. Summary

In conclusion, the thermo-optic characteristics of active photonic crystal structures on an SOI platform are investigated semi-analytically. The power consumption Q_π and spatial temperature profile are given as explicit functions of structural, thermal, and optical parameters. The results agree well with FEM simulations and also explain the low switching power in air-

bridge structures. The scaling of Q_π with key physical parameters is analyzed. The practical limit of Q_π is estimated on the sub-milliwatt level considering all key factors.

Acknowledgements

The odd mode research is completed in collaboration with Drs. Ming Lu and Aaron Stein of the Center for Functional Nanomaterials, Brookhaven National Laboratory. The thermo-optics research is completed in collaboration with Prof. George K. Celler and Yogesh Jaluria of Rutgers University. We are grateful to Prof. S. R. McAfee for helpful discussions. Manjit Chahal is supported by a Rutgers ECE Graduate Fellowship.

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11 Large area single crystalline silicon nanomembrane fabrication for MMI structure

John Rogers

Our main accomplishment has been the development of effective transfer printing method of large area silicon nanomembranes for vertical integration of photonic components. Size of nanomembrane (2.05 mm x 8.05 mm) has increased to realize the printed second layer 1 x 12 multimode interference (MMI) coupler and optimum fabrication process of those large area nanomembranes has been established. For the assembly of double-layer nanomembrane device, retrieval and printing processes of fabricated nanomembrane inks have been also optimized to achieve crack-free printing of large area nanomembrane on the first layer MMI coupler. The resulting photonic device has shown uniform output of guided light (wavelength of 1550 nm) on both the first and the second layer MMI coupler devices with low insertion loss.

11.1 Large area single crystalline silicon nanomembrane fabrication for MMI structure

Figure 1 provides a process flow for the fabrication of large area silicon nanomembrane inks. Silicon nanomembrane sheets with rectangular shape (2.05 mm x 8.05 mm) were defined by patterning 230 nm-thick silicon device layer of SOI wafer with photolithography and reactive ion etching (RIE) processes. Exposed buried oxide (BOx) layer (thickness ~ 1 um) was partially undercut by dipping in concentrated HF (49%) for 55 sec and photoresist support was introduced along the perimeter of individual nanomembranes. Full undercut etching of BOx layer left inside the photoresist support was carried out in concentrated HF (49%) for 19 hrs, which resulted in the releasable structure of nanomembrane that was tethered to the photoresist support. Note that the resulting nanomembrane inks should be washed with plenty of deionized water after taking out of HF and then fully dried in the atmosphere at least for 2 days to remove residual HF in nanomembrane; residual HF in nanomembrane caused PDMS stamp to be partially dissolved/damaged and made nanomembrane bonded to surface of PDMS stamp when stamp was made a contact with nanomembrane in retrieval step, resulting in the failure in printing step.

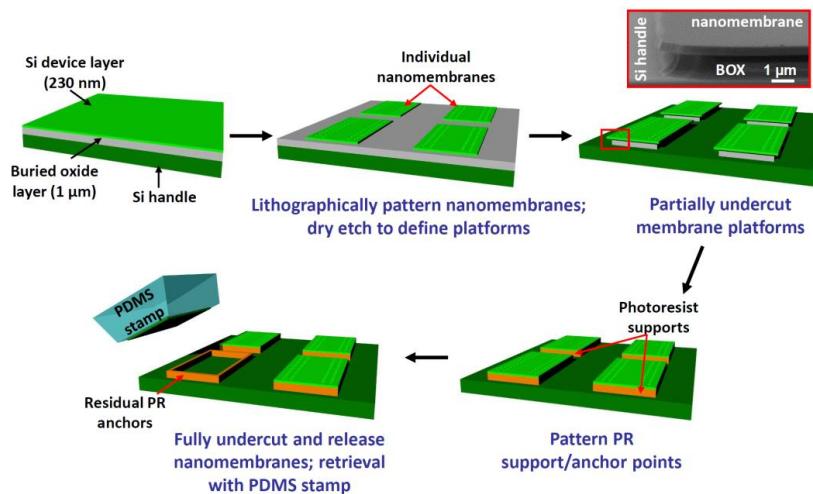


Figure 1. Fabrication process of large area silicon nanomembrane ink.

11.2. Transfer printing of silicon nanomembranes on the first layer MMI coupler

Figure 2(a) shows an illustration of assembly process for the fabrication of double-layer 1 x 12 multimode interference (MMI) coupler by stacking silicon nanomembrane layer through transfer

printing and patterning steps. The first layer MMI coupler device was provided by University of Texas; for the fabrication of the first layer MMI coupler, silicon device layer of commercially available SOI wafer (250 nm silicon device layer, 3 μm buried oxide layer) was defined by electron beam lithography (EBL) and subsequent RIE processes. On the first layer MMI coupler, we deposited 1.5 μm -thick silicon dioxide layer that serves as interlayer dielectric between the first and the second nanomembrane layers by plasma enhanced chemical vapor

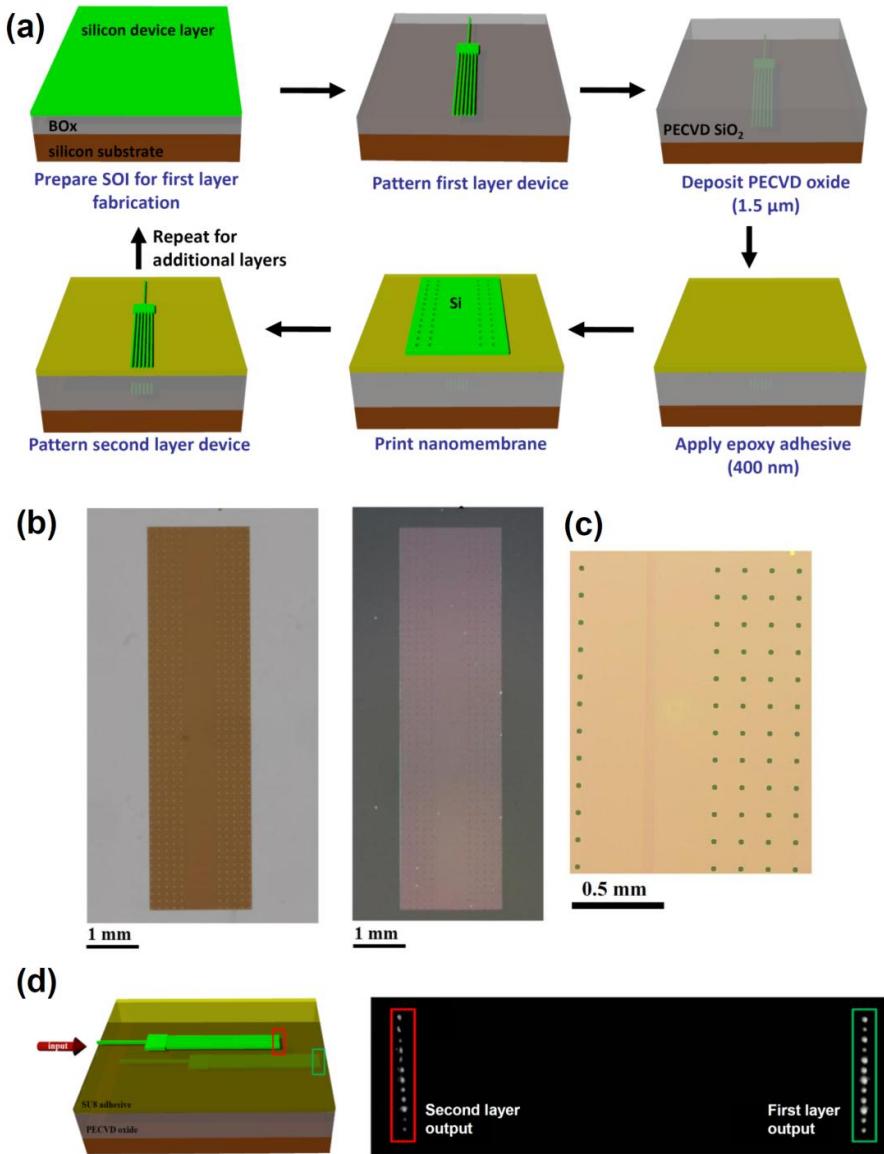


Figure 7. (a) Schematic process flow for assembling double-layer device using printed silicon nanomembranes for the second layer devices. (b) Photograph images of silicon nanomembrane on the stamp after retrieval (left) and printed nanomembrane on the first layer device (right). (c) Optical microscope image of printed, crack-free nanomembrane. (d) Schematic illustration of separated waveguide outputs of the first and the second layers (left) and a top-down IR image of two 1 x 12 MMI couplers with simultaneous excitation in both layers.

deposition (PECVD) method. To facilitate the transfer printing of the second layer silicon nanomembrane, photocurable epoxy adhesive (thickness ~ 400 nm, SU-8) was spin cast on the silicon dioxide surface, baked at 95°C for 60 sec, and activated by flood UV exposure.

For transfer printing of the second layer nanomembrane, silicon nanomembrane ink was retrieved by a PDMS stamp mounted to a rigid glass backing. Left image of Figure 6(b) shows a single silicon nanomembrane on the surface of the stamp after retrieval. The inked PDMS was aligned and brought into contact with the photo-activated adhesive surface using custom alignment/tilting adjustment equipment that is integrated with heating platform. While in contact, adhesive was fully cured by heating at 70°C for 10 minutes. After the curing, transfer printing of nanomembrane for the second layer device was completed by slowly retracting the stamp (~500 um/s) from the surface of nanomembrane. Right image of Figure 6(b) shows a printed silicon nanomembrane. Note that the central region of printed nanomembrane (the region without etch holes) should be crack-free to achieve the continuous waveguide structure as shown in Figure 6(c). Cracks in nanomembrane are normally induced by expansion (or stretching) of elastomeric PDMS. Therefore, lamination of stamp to nanomembrane without pressing during retrieval step and tilting adjustment of stamp to avoid the large deformation of stamp during making a contact between the inked PDMS and the substrate are critical factors to obtain the crack-free printed nanomembranes. Device stack with the printed second layer was sent back to University of Texas and the second layer MMI coupler with the printed nanomembrane was fabricated using the same EBL and RIE processes as the first layer MMI coupler fabrication. Figure 6(d) shows the results of simultaneous excitation of two MMI couplers on both layers, demonstrating uniform output of guided light on both the first and the second layers with low insertion loss.

12 Lithography for silicon nanomembranes

R. Fabian Pease, PI

Overview

Originally, Stanford's lithographic research results would be used to realize UT's 3-D optical phased array (OPA) system. But Stanford's acquisition of an ASML 5500 stepper with ASML committed to maintaining it as their West Coast demonstration unit provided all the lithography capability needed for the OPA.

Multi-level planar waveguide arrays for the 3-D OPA

This was reported in considerable detail at the November review. Fabrication of single and double layer planar waveguide arrays with co-fabricated heater elements continues. The fabrication flow is shown in figure 1. From previous study the optimal starter material was determined to be commercial SOI because of the tightly controlled total thickness variation (TTV) of less than 20nm across a 150mm wafer and the low roughness of the silicon device layer. The roughness of the device layer must be low to allow device bonding and to limit optical loss in the silicon waveguide. We have replaced traditional silicon fusion bonding with a bonding process based on spin on glass. This greatly relieves the necessary roughness and wafer flatness requirements for bonding, in addition, to eliminating the need for surface preparation.

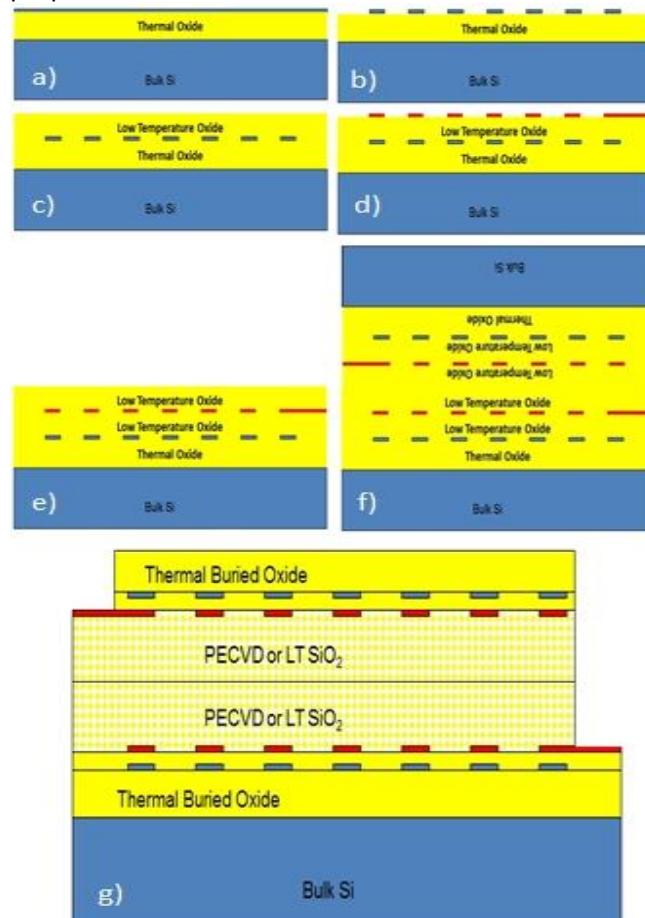


Figure 1: Process flow for fabricating a multi-layered photonic lightwave circuit. From (a) the initial starting material is patterned (b) to define the waveguides. Then (c) these waveguides are isolated optically by thick SiO_2 deposition. Next (d) metallic heater electrodes are patterned and (e) thermally isolated by thick SiO_2 . Two system (f) are bonded together and then (g) one of backing wafers is removed by etching.

Stochastic waveguide roughness analysis

Effect of Deterministic surface roughness on optical waveguide performance

In an effort to understand the effect of line edge roughness on silicon waveguides, we have patterned waveguides with built in roughness levels. This roughness is defined by high resolution ebeam lithography and transferred into the silicon layer with reactive ion etching to preserve the pattern as

accurately as possible. A range of designed, artificially roughened waveguides are shown in Figure 2. The ebeam lithography system allows resolution on the order of 10nm, which is just a few percent of the waveguide design thickness.

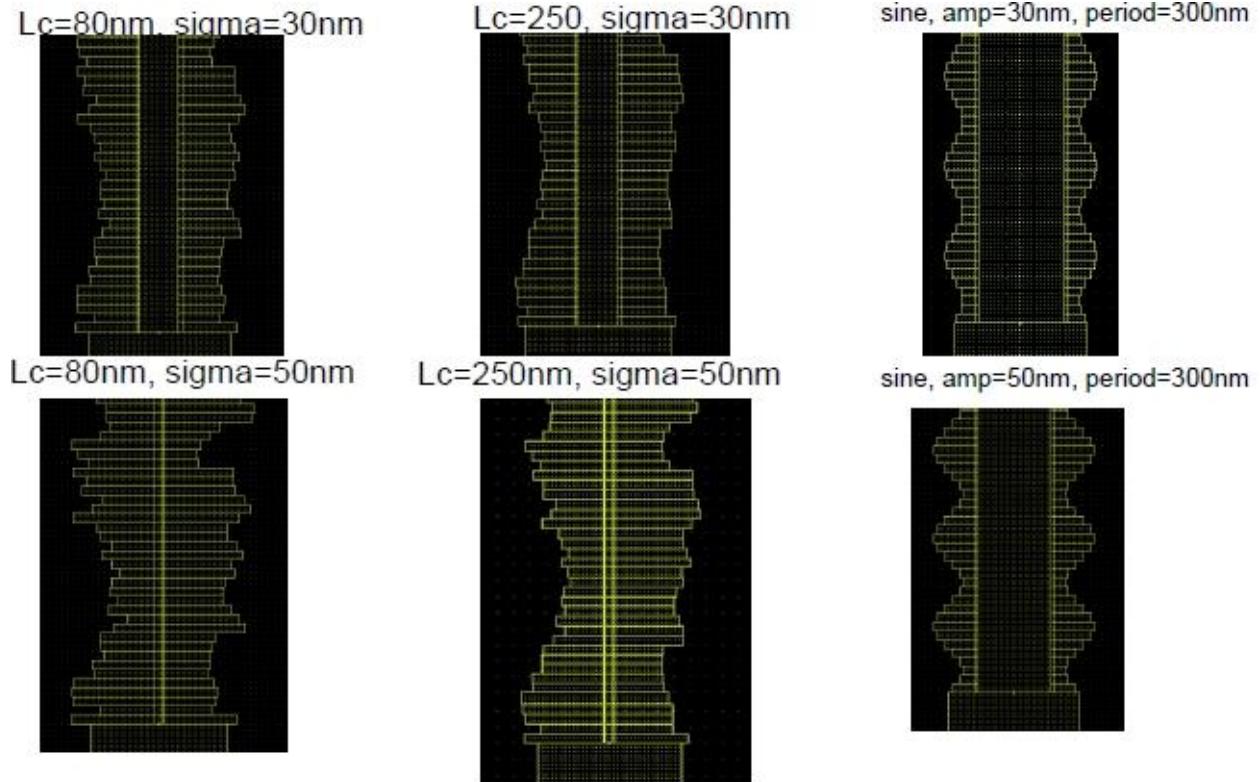


Figure 2: Layout patterns for ebeam lithography showing a few of the designs for directed roughening of silicon waveguides. The loss for different altered waveguides will be analyzed to determine the effect of line edge roughness in the system.

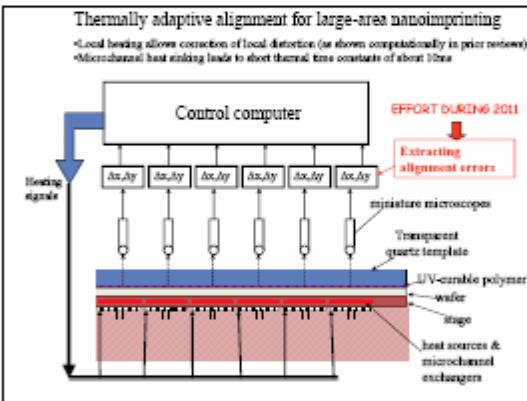
Lithography for silicon nanomembranes

Stanford University Team:

R. Fabian Pease, PI
 J. Provine, Senior Research Associate
 Euclid Moon, Visiting Research Scientist (from MIT)
 Yao-Teh Cheng, PhD Candidate

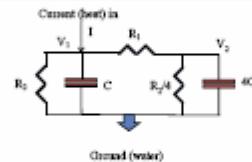
Plan Evolution

- Originally, Stanford's lithographic research results would be used to realize UT's 3-D optical phased array (OPA) system
- But Stanford's acquisition of an ASML 5500 stepper with ASML committed to maintaining it as their West Coast demonstration unit provided all the lithography capability needed for the OPA.
- So lithography research is concentrating on thermally adaptive alignment for large-area nanoimprinting.
- Stanford's other capabilities being used for realizing the 3-D OPA. In particular the capability of attaching single crystal islands of silicon to SiO_2 films was developed as part of the 3-DIC project.
- Stanford is now providing starting wafers, lithography and etching of Si waveguides, deposition of SiO_2 and heater metal, lithography and etching of heater metal, planarizing deposited SiO_2 surfaces, bonding, and etching back upper level structures. These completed structures are then sent to UT for integration into the OPA.



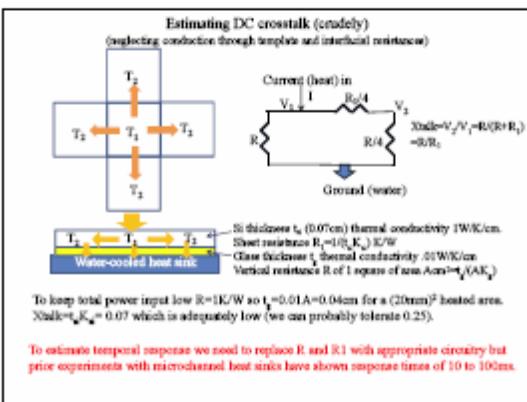
Lumped Thermal Model

Equivalent circuit for selective heating



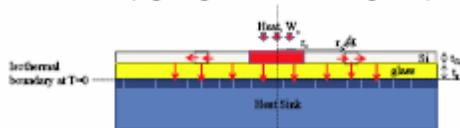
*With a water-cooled microchannel heat sink thermal time constants, τ_{th} , of between 10 and 30ms have been demonstrated with practical interface.

Need high R_2 (downs through wafer) to avoid crystallization advantages to membranes.



Continuous Model

(neglecting heat conduction through mask)



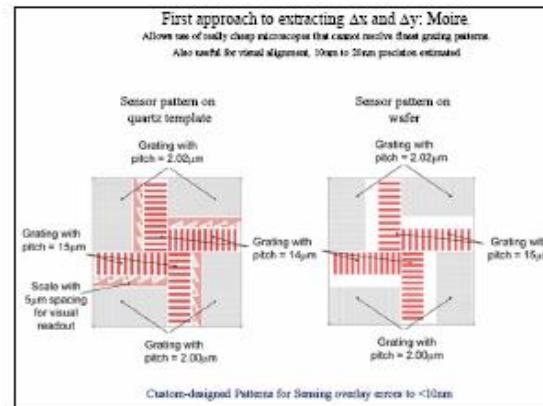
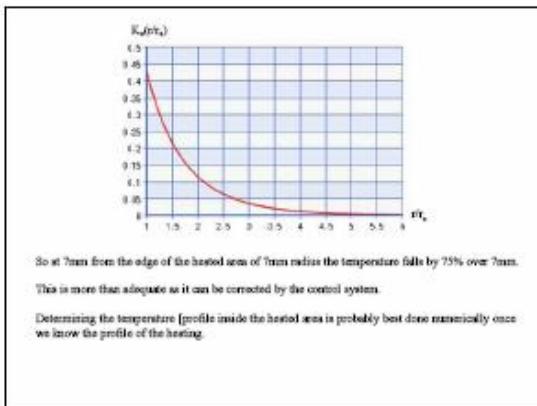
Crosstalk is set by how fast T bulk decreases as z increases.

For now, T can be found by solving one of the Bessel equations:

$$T'' + T'/k - Dr_z^2 T = 0 \quad \text{where } ' \text{ denotes } d/dz \text{ and } '' \text{ denotes } d^2/dz^2$$

The solution is $T=T_0 K_0(\mu z/\sqrt{k})$ where K_0 is a modified Bessel function of the second kind

And $\mu = \sqrt{\pi k_1 K_0 K_1}$. For $K_0 = 1\text{W/cmK}$, $K_1 = 0.01\text{W/K/cm}$, $t_s = 0.7\text{mm}$, $t_g = 7\text{mm}$.

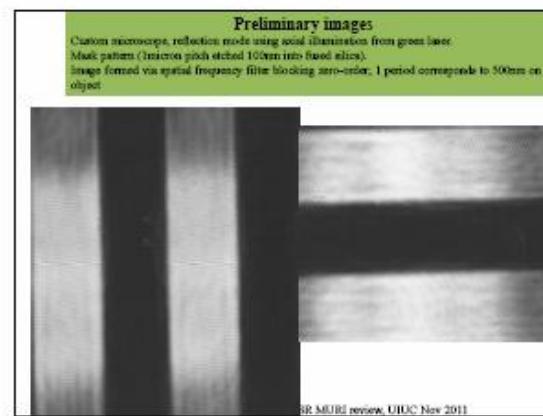
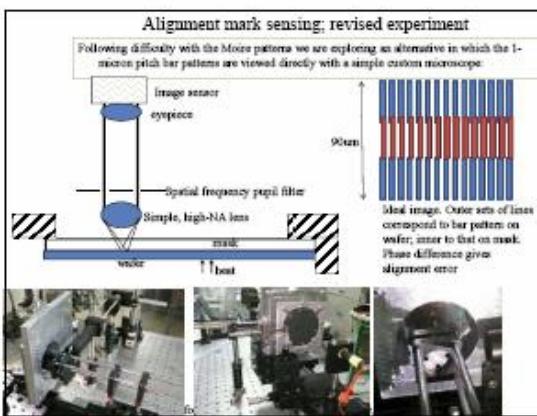


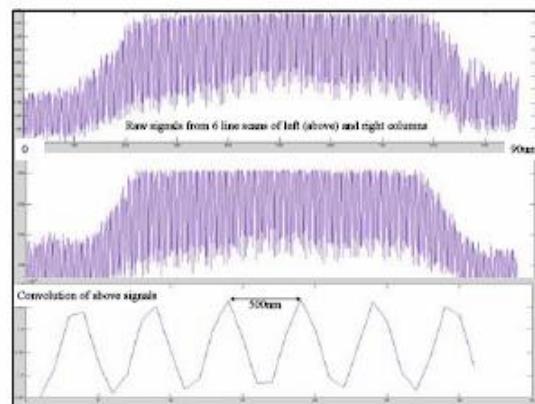
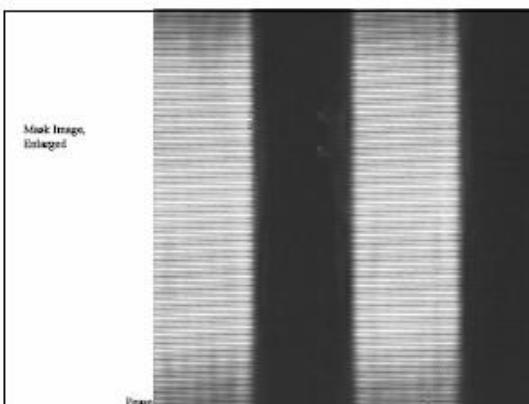
Second approach to extracting Δx and Δy :
Direct viewing of patterns followed by intensive computation

- Difficulty obtaining adequate contrast with Moire technique because of index matching of interfacial oil and nanoinprint alignment marks
- Need less cheap microscopes that can resolve finest patterns and are thin enough to allow an array of them and space for the exposing excimer laser pulse (for SFIL). A 20mm diameter microscope can easily resolve 1 micron pitch grating (using a CMOS image sensor array).
- Looking at simple grating patterns corrupted by noise, and featuring variable contrast, resolution, line edge roughness and undesired Moire effects through beating with the image sensor array (there might be ways of exploiting this last effect).
- Initial results promising. Precision to 1/100 of period appears feasible (10nm for 1micron pitch grating)
- Variety of computing algorithms tested.

Position sensing (1-D)

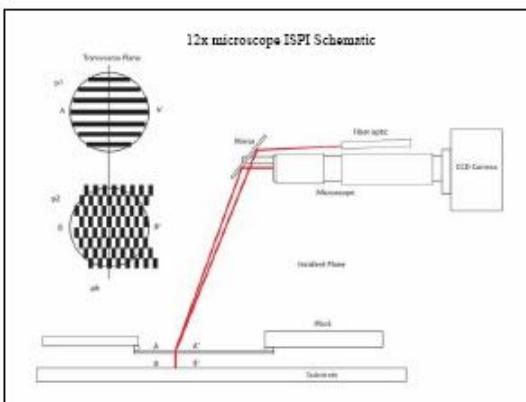
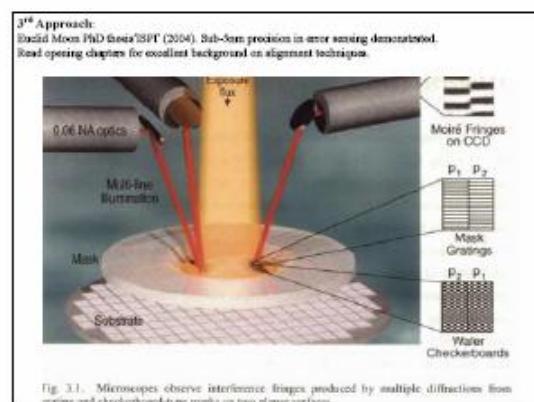
- In the absence of noise just 1 edge can give unlimited precision. Maybe useful to bear in mind (e.g. sub-pixel precision is possible) but practically irrelevant.
- To maximize the signal interrogate as many edges (suitably oriented) as possible before losing (too much) contrast. I picked 1-micron pitch grating on the wafer and on the mask.
- To minimize noise just select the useful spatial frequencies and compare phases from wafer and mask images. Simple pupil filter with four openings has been a good start.
- Use computation for subsequent signal processing

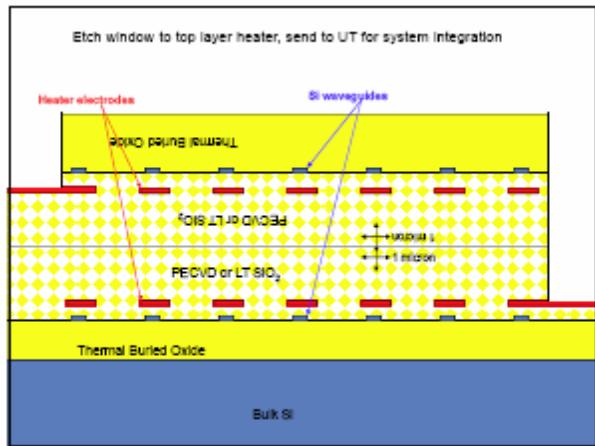




Status as of June 2012

- Overlay error sensing using straightforward grating patterns looks promising. 10nm precision looks doable.
- Not clear how far computation can replace optical engineering. For example how much spatial frequency filtering should be done optically. The pupil filter is appropriate as it is both effective and easy to implement. The weaker mask signal can be separately amplified to match the wafer signal.
- Local thermal management still to be characterized but present experimental arrangement should suffice (modification needed for better mechanical adjustment of wafer on mask, for cleaner illumination and eliminating 120Hz interference). May well be more useful initially for membrane overlay than for IC processing.
- Moiré techniques now being re-visted with Euclid Moon as a visiting scholar to Stanford. Experimental arrangement nearing completion.





13 High-Q Resonances From Si-nanomembrane Based MMs Gennady Shvets

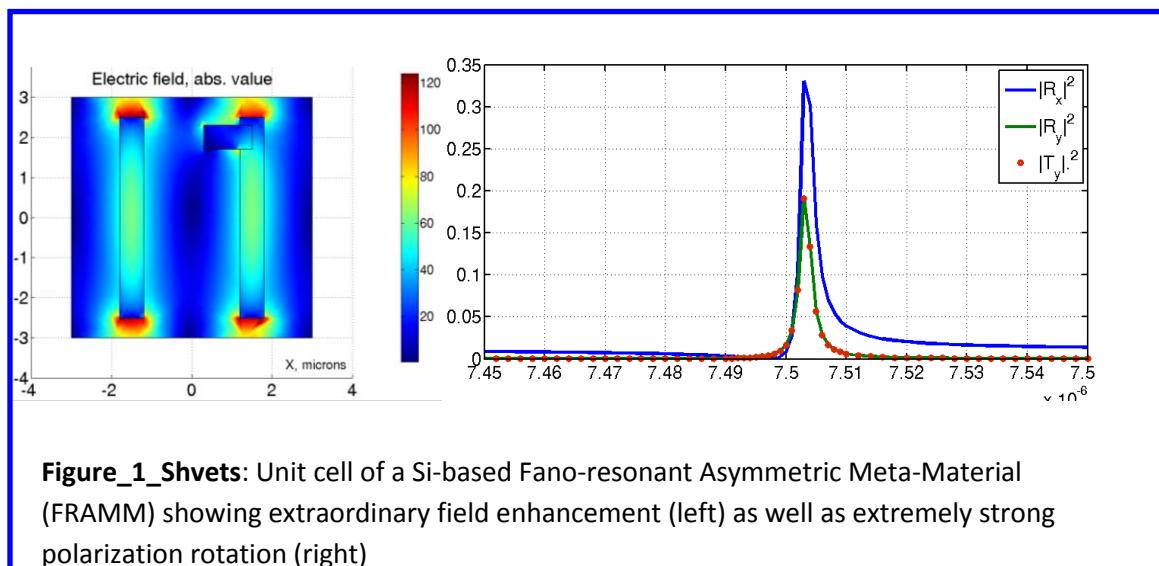
During the past year our group concentrated on developing high-Q metamaterials based on Si membranes. This work is motivated by high losses in plasmonic metamaterials. These losses compel us to seek alternatives. We have identified one such alternative: Si-based metamaterials. Crystalline property of Si is essential to making high-Q metamaterials that can be attractive as nonlinear optics devices, Stokes parameter polarimeters, and biosensors. This work has three components: theoretical/computational, fabrication (in collaboration with SNL), and optical characterization.

Three students were partially supported using this grant:

1. Mr. Chih-Hui Wu (graduate student)
2. Mr. Nima Dabidian (graduate student)
3. Mr. Nihal Arju (graduate student)

13.1 Theory: Extraordinary Field Enhancements and High-Q Resonances From Si-nanomembrane Based MMs

Modeling results shown in Figure 1-Shvets illustrate the concept: we can use Si metamaterials to generate extremely high field enhancements. Because this metamaterial is highly asymmetric, one of the possible experimental signatures could be polarization rotation shown in Fig.1-Shvets (right).



The best platform for making such antennas is SOI nanomembranes, where buried oxide can serve as the etch stop for making Si metamaterials.

13.2 Fabrication using SOI nanomembranes as the platform

The wafer used for Si fabrication was double silicon-on-oxide type. The top silicon thickness varies between 1.2-1.5 microns according to cross section scanning electron microscope image shown below.

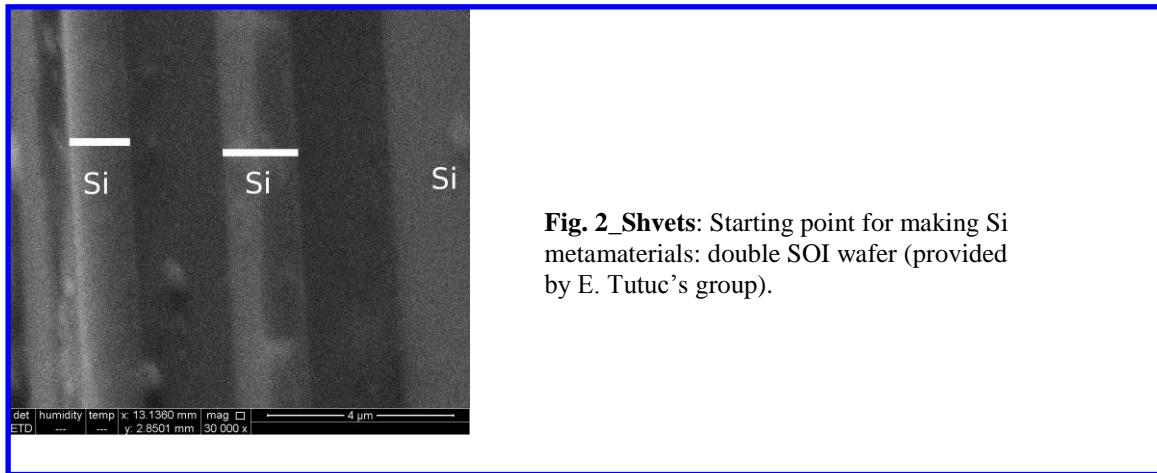
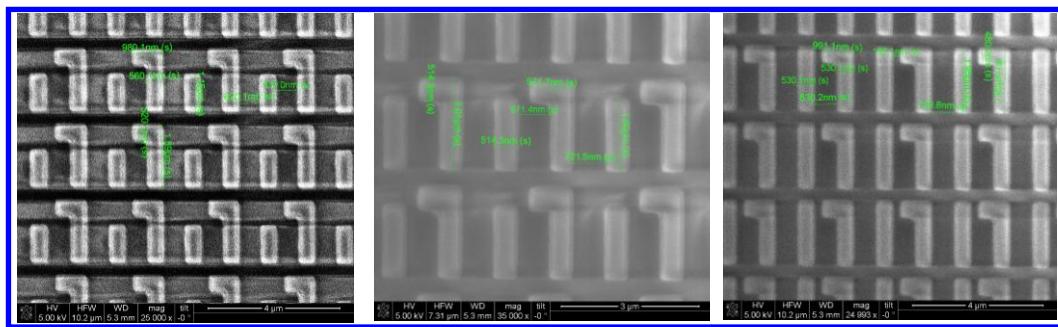


Fig. 2_Shvets: Starting point for making Si metamaterials: double SOI wafer (provided by E. Tutuc's group).

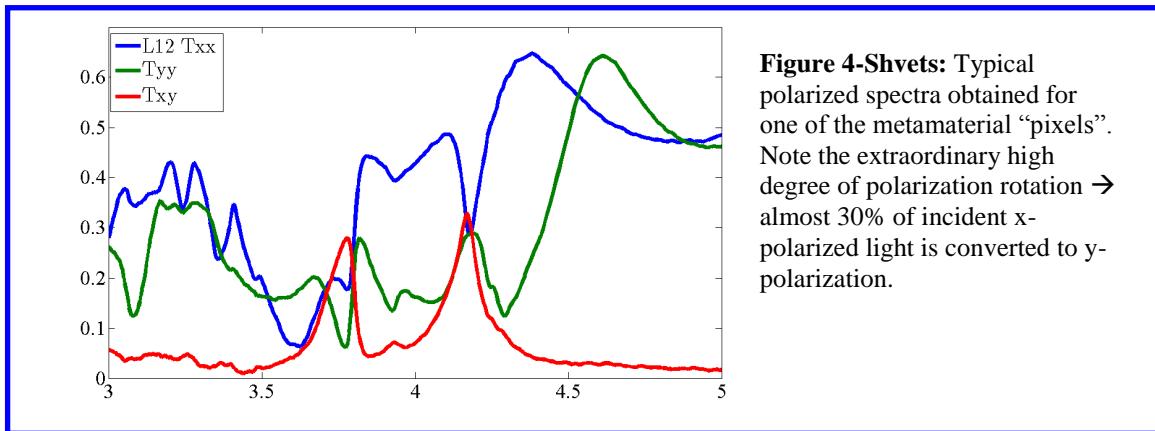
The sample was first patterned using an electron beam lithography system using NEB (negative) resist. Then it was dry etched with the following parameters ICP/Bias – 300W/25V, pressure 15mTorr, Ar flow 40 sccm, HBr flow at 15sccm, temperature 60C.

Typical dimensions of the fabricated structures: the longer antenna is 2 μm long, and the short antenna is 1.2 μm long. We made an array of the unit cell shown above with a periodicity of 2.4 μm in both X and Y direction. We made several samples with different length of the shorter antenna. The longer antenna was kept at 2 um long, and the shorter antenna was varied in order to control the degree of symmetry breaking and thereby coupling with propagating modes. This allows us to control the quality factor of the quadrupole resonance of these structures. The following are the SEM pictures of three representative arrays of silicon pi structures.



13.3 Optical characterization of Si-based FRAMMs using FTIR (normal incidence)

Transmission at normal incidence was obtained using house-built angle-resolved FTIR setup. For the L12 sample (short antenna is 1.2 μm long), the normal transmission spectrum is shown in Fig.4-Shvets, where T_{xy} stands for “y-polarized transmission of the incident x-polarized radiation”.



It is notable that the cross polarized transmission T_{xy} is in excess of 30% for quadrupole resonance. Presently we are investigating the possibility of making a highly-efficient circular polarizer based on Si nanomembrane metamaterials.

14 Conclusion

In summary, during this period of MURI program, our team has continued our monthly meeting and significant progresses have been made on both optical phased array (OPA) using actively tuned unequally spaced nano-waveguide arrays and optical true time delay (TTD) devices using photonic crystal waveguides where are all made on silicon nanomembranes. Integrated photonic circuit including 1x12 multimode interference (MMI) coupler, 12 waveguide adiabatic tapers, 12 thermal optical phase tuners, 12 delay lines and 12 non-equally spaced optical faced arrays are fully integrated on a silicon nano-membrane. The device is fully-packaged and tested. The problem of far field inside a silicon slab has been formulated. Beam steering over 30 degrees has been experimentally confirmed.

An ultra-compact polarization splitter has been demonstrated using a Two Mode Interference (TMI) couplers that also has large fabrication tolerance. Polarization splitters are key components for photonic integrated circuits consisting of polarization dependent devices.

The use of polycrystalline silicon for multi-layer photonic integration has been investigated, and the loss mechanisms due to grain boundaries have been explored. Not only do we show that wide multimode waveguides can be made with low loss contrary to previous reports, but we also present the polysilicon waveguides with the lowest loss to date. Furthermore, we demonstrate the feasibility of polysilicon as a multilayer photonic material by using a low loss and high uniformity 1x12 MMI.

We have also continued our study on self-alignment by patterning multi-bonded SOI wafers. This approach includes bonding doped/undoped silicon nanomembrane and silicon dioxide layers of arbitrary thicknesses. Using double-bonded SOI, we have demonstrated double layer 1x12 MMIs fabricated using a single etch step that has low excess loss and high uniformity for both silicon layers.

We further demonstrated and refined a rate-dependent printing procedure which utilizes simple line and space molded relief features patterned in an elastomeric stamp surface to facilitate easier transfer between substrates. Basic capabilities including optimized nanomembrane design and fabrication have been demonstrated. We have also investigated the assembly of these large area Si nanomebranes as active components for optical phase array waveguides. New automated transfer printing tool bits have been developed to facilitate high precision printing of three dimensional stacks of nanomembrane-based devices. This has allowed us to realize a double layer 1x12 MMI using standard SOI as the starting substrate, and then printing a silicon nanomembrane sheet above it for second layer patterning. Efforts are underway to further characterize and improve the optical performance of this printing method.

In an effort to improve the coupling efficiency from end-fire coupling for coupling light from fibers to photonic circuits, we have explored several fiber to chip coupling methods. Using subwavelength grating couplers for out of plane coupling, we demonstrate high coupling efficiencies with modest bandwidth. Efforts are continually underway to improve both the coupling efficiency and the bandwidth. We have also explored on-chip spot size converters for in-plane coupling, also with high coupling efficiencies and also high bandwidth.

Further delay time exploration for optical-true-time-delay using photonic crystal waveguides is also investigated, including high coupling efficiency into the slow light slotted photonic crystal waveguides by means of mode converters and index matching tapers. In addition, a 4 channel on-chip true time delay using photonic crystal waveguides is demonstrated, with group index as high as 23 without significant loss. A steering angle of 45 degrees for X-band PAA is possible.

15 Major Publications in this period

Journal Papers

- 1 Yang Zhang, Amir Hosseini, Jaehyun Ahn, David N. Kwong, Babak Fallahazad, Emanuel Tutuc, and Ray T. Chen, "Vertically integrated double-layer on-chip silicon membranes for 1-to-12 waveguide fanouts," *Appl. Phys. Lett.* 100, 181102 (2012)
- 2 Che-Yun Lin, Alan X. Wang, Wei-Cheng Lai, John L. Covey, Swapnajit Chakravarty, and Ray T. Chen, "Coupling loss minimization of slow light slotted photonic crystal waveguides using mode matching with continuous group index perturbation," *Opt. Lett.* 37, 232-234 (2012)
- 3 Che-Yun Lin, Harish Subbaraman, Amir Hosseini, Alan X. Wang, Liang Zhu, and Ray T. Chen, "Silicon nanomembrane Based Photonic Crystal Waveguide Array for Wavelength-Tunable True-Time-Delay Lines," to appear in *Applied Physics Letters*
- 4 Hosseini, S. Rahimi, X. Xu, D. Kwong, J. Covey, and R. T. Chen, "Ultracompact and Fabrication-Tolerant Integrated Polarization Splitter," *Optics Letters*, vol. 36, no. 20, pp. 4047-4049, 2011
- 5 D. Kwong, A. Hosseini, Y. Zhang, R. T. Chen, 1x12 Unequally-spaced Waveguide Array for Actively-tuned Optical Phased Array on a Silicon Nanomembrane, *Applied Physics Letters*, Vol. 99, pp. 051104, 2011
- 6 D. Kwong, J. Covey, A. Hosseini, Y. Zhang, X. Xu, R. T. Chen, "Ultralow-loss polycrystalline silicon waveguides and high uniformity 1x12 MMI fanout for 3D photonic integration," to be submitted to *Optics Express*.
- 7 Xiaochuan Xu, Harish Subbaraman, John Covey, David Kwong, Amir Hosseini, and Ray T. Chen, "CMOS Compatible High Efficiency Subwavelength Grating Couplers for Silicon Integrated Photonics," to appear in *Applied Physics Letters*
- 8 1. Jun Tan, Ming Lu, Aaron Stein, and Wei Jiang, "High purity transmission of a slow-light odd mode in a photonic crystal waveguide," *Opt. Lett.* (accepted).
- 9 2. M. Chahal, G. K. Celler, Y. Jaluria, and W. Jiang, "Thermo-optic characteristics and switching power limit of slow-light photonic crystal structures on a silicon-on-insulator platform," *Opt. Express*, vol. 20, 4225-4231 (2012).

Conference Papers

- 1 C.-Y. Lin, A. Hosseini, H. Subbaraman, Z. Xue, A. Wang, R. T. Chen, "Wavelength-Tunable on-Chip True Time Delay Lines Based on Photonic Crystal Waveguides for X-Band Phased Array Antenna Applications," CLEO 2012 Proceedings of the Conference on Lasers and Electro-Optics CTu3I.7 (2012)
- 2 Y. Zhang, A. Carlson, S. Y. Yang, A. Hosseini, D. Kwong, J. Rogers, R. T. Chen, "Double-layer Photonic Devices Based on Transfer Printing of Silicon Nanomembranes for Three-dimensional Photonics," CLEO 2012 Proceedings of the Conference on Lasers and Electro-Optics CTu1A.5 (2012)
- 3 D. N. Kwong, J. Covey, A. Hosseini, Y. Zhang, R. T. Chen, "Feasibility of Multimode Polycrystalline Waveguides/Devices: Record Low Propagation Loss and Uniform 1x12 MMI Fanout," CLEO 2012 Proceedings of the Conference on Lasers and Electro-Optics CM3A.2 (2012)
- 4 Y. Zhang, A. Hosseini, J. Ahn, D. N. Kwong, B. Fallahazad, E. Tutuc, R. T. Chen, "Double-layer 1x12 Multimode Interference Coupler for Three-dimensional Photonic Integration," IEEE Optical Interconnects Conference, paper TuD4, 2012

- 5 (Invited) Zhiping Zhang, Chien-Yu Chen, Filip Crnogorac, Peter Griffin, Fabian Pease, James Plummer and Simon Wong, "Monolithic 3D Integration" **Conference Papers presented at EIPBN2012**
6. F. Crnogorac*¹, R. Birringer², R. Dauskardt², R.F.W. Pease, "Monolithic 3D Integration via Al-Ge Bonding of Single Crystal Islands," **Conference Papers presented at EIPBN2012**
- 7.(Invited) J Provine¹, Filip Crnogorac³, David Kwong², Ray T. Chen², R. F. W. Pease,"Transfer Processes of Silicon Nanomembranes for Three Dimensional Integration of Photonics and Electronics", **Conference Papers presented at EIPBN2012**
8. Ryan A. Integlia, Lianghong Yin, Duo Ding, David Z. Pan, Douglas M. Gill, Weiwei Song, Ying Qian and Wei Jiang, "Fabrication and characterization of parallel-coupled dual racetrack silicon microresonators," *Proc. SPIE* 8266, 82660M (2012).
- 9 Weiwei Song, Ryan A. Integlia, and Wei Jiang, "Slow Light Loss Due to Roughness in Photonic Crystal Waveguides: Insights on Loss Reduction from an Analytic Theory," *Photonics West*, San Jose, CA, January 2012.
- 10 Weiwei Song, Jun Tan, Ryan Integlia, Lianghong Yin, and Wei Jiang, "Ultra-High Sensitivity in a Photonic Crystal Superprism Due to the Curvature Singularity of a Dispersion Surface," *IEEE Photonics Conference*, Washington, DC, October 2011.